Design of an Impedance Source Converter for High-Performance PV Power System Applications

- EE6 - Electrical Engineering -

Project Report

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Abstract:

This project describes the principles of impedance-source/quasi-impedance-source inverters, which have the main particularity of being able to operate as voltage-boost inverters. Therefore, the appropriate circuit analysis and modelling are presented, together with a study of the control methods applicable to this type of inverters. The design of passive components to meet electrical requirements is also presented. Theoretical results are validated with both circuit simulations and experimental tests.

The content of this report is freely available, but publication (with reference) may only be pursued due to agreement with the author.

Nomenclature

Symbol	Description	SI Unit
a	Peak-to-peak ripple ratio of the DC-link voltage.	/
b	2ω current ripple ratio of the inductors.	/
B	Boost factor of the qZSI.	/
C_1	First capacitor in the Z-source network.	F
C_2	Second capacitor in the Z-source network.	F
D	Shoot-through duty ratio.	/
G	Voltage gain of the qZSI.	/
i_{ac}	Current at the AC side of the inverter bridge.	A
I_{ac}	Peak current at the AC side of the inverter bridge.	A
I_{C1}	DC current through C_1.	A
I_{C2}	DC current through C_2.	A
I_D	DC current through the qZSI diode.	A
I_{in}	DC current supplied by the power source of the qZSI.	A
$\tilde{i}_{L1}$	2ω current ripple of i_{L1}.	A
$\tilde{i}_{L2}$	2ω current ripple of i_{L2}.	A
I_{L1}	DC current through L_1.	A
I_{L2}	DC current through L_2.	A
I_{PN}	Current at the DC side of the inverter bridge.	A
L_1	First inductor in the Z-source network.	H
L_2	Second inductor in the Z-source network.	H
M	Modulation index of PWM control.	/
P	Power rating of the system.	W
Q_n	Switching devices of the inverter bridge ($n = 1, 2...6$).	/
T_{nsh}	Time interval of the non-shoot-through state.	s
T_s	Time interval of one switching cycle.	s
T_{sh}	Time interval of the shoot-through state.	s
T_z	Working time interval of V_z.	s
$T_{0,1...7}$	Working time intervals of $V_{0,1...7}$.	s
$\vec{V}$	Rotating space vector voltage reference for SVM.	V
V_a	Phase to neutral voltage of phase a.	V

Symbol	Description	SI Unit
v_{ac}	Voltage at the AC side of the inverter bridge.	V
$\hat{v}_{anm}$	Amplitude of m-th harmonic of phase a.	V
V_{ac}	Peak voltage at the AC side of the inverter bridge.	V
$\hat{v}_{an1}$	Fundamental amplitude of the AC voltage of phase a.	V
V_b	Phase to neutral voltage of phase b.	V
$\hat{v}_{bn1}$	Fundamental amplitude of the AC voltage of phase b.	V
V_c	Phase to neutral voltage of phase c.	V
$\hat{v}_{cn1}$	Fundamental amplitude of the AC voltage of phase c.	V
V_{C1}	Voltage across C_1.	V
V_{C2}	Voltage across C_2.	V
V_{diode}	Voltage across the qZSI diode.	V
V_{in}	Input voltage of the qZSI.	V
v_{L1}	Voltage across L_1.	V
v_{L2}	Voltage across L_2.	V
V_n	Lower reference voltage for carrier-based qZSI PWM.	V
V_{out}	Output voltage of the qZSI.	V
V_p	Upper reference voltage for carrier-based qZSI PWM.	V
V_{PN}	DC-link voltage across the inverter bridge.	V
V_s	DC input voltage.	V
V_{sine}	Amplitude of the sinusoidal reference for PWM.	V
V_T	Triangular wave amplitude for carrier-based qZSI PWM.	V
V_{tri}	Amplitude of the triangular carrier wave for PWM.	V
v_x	x-axis voltage in the x-y coordinate system.	V
v_y	y-axis voltage in the x-y coordinate system.	V
V_z	Combination of the zero reference vectors V_0 and V_7.	V
$V_{0,1...7}$	SVM reference voltage vectors.	V
δi_{L1}	Current ripple of i_{L1}.	A
δi_{L2}	Current ripple of i_{L2}.	A
δT	Time interval of the division of T_{sh} by the control method.	s
δv_{C1}	Voltage ripple of v_{C1}.	V
δv_{C2}	Voltage ripple of v_{C2}.	V

Symbol	Description	SI Unit
θ	Angle between V_1 and $\vec{V}$.	rad
θ_k	Sector angle of the reference vector $\vec{V}$.	rad
ϕ	Phase angle at the AC side.	rad

Contents

Preface

This project has been completed within the Aalborg University Electrical Energy Engineering programme by two sixth semester exchange students from the Beijing Institute of Technology, Beijing and the Polytechnic University of Catalonia, Barcelona. The project has been written in the period of the 6th of February to the 8th of June in 2018.

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Summary

This project report analyzes the impedance source inverter as a means to improve the performance of PV systems over existing inverter topologies, by allowing voltage-source inverters to boost output voltage. To do so, an impedance network is inserted between the voltage source and the inverter legs. Many different topologies have been suggested for such an impedance network (also referred to as a Z-source network), and all of them share the use of inductors, capacitors, and either diodes or transistors.

The Introduction chapter of the presented report contextualizes the study of inverters as a fundamental element of PV power systems. It then briefly introduces the main traditional converter topologies, after which the principles of the impedance source inverter are presented. Essentially, the impedance source network allows for one or several inverter legs to be short-circuited by gating on both the upper and lower switching devices simultaneously, a forbidden state in most voltage-source inverter topologies, and allowing the Z-source network to store energy during these shoot-through states. This stored energy is then discharged during the non-shoot-through states, consequently boosting the DC-link and output voltages.

Several topologies of impedance source networks are presented, each aiming to improve one or several aspects of the original impedance-source proposed by F. Z. Peng in 2003. The presented project focuses on the quasi-impedance-source inverter, or qZSI, which is one of the most widespread topologies of impedance source inverter, as it allows a continuous DC input current without modifying the basic components of the original impedance source; while also providing a common DC rail between the voltage source and the inverter legs.

The next chapter is focused on the analysis of the qZSI. Starting with the steady-state circuit analysis of the qZSI, the DC components of its main parameters can be deduced, focusing especially on the output voltage, inductor current, and capacitor voltage; and illustrating the working principles of the impedance source inverter.

The final part of the chapter focuses on the design of the passive components of

the impedance network. To do so, the ripple components of the main parameters of the three-phase qZSI are calculated. The development of the complete model of the single-phase qZSI is also included.

Afterwards, the main open-loop control techniques used for the qZSI are presented. In terms of modulation strategies, there are mainly two pulse-width modulation (PWM) control methods: carrier-based PWM and space vector PWM. The principles of both modulation techniques are explained, focusing first on their variants for traditional three-phase inverters. Afterwards, several methods to insert the shoot-through states are introduced, with three methods for the carrier-based PWM and four for the space vector PWM. Finally, all the discussed modulation methods are compared.

The next chapter focuses on the experimental tests, first describing the experimental setup, which is based on the qZSI topology. Two control methods are tested in the experiments, the carrier-based PWM simple boost control and the space vector PWM ZSVM6, which divides the shoot-through states into six equal parts and evenly inserts them into all six switching control signals. Three data series are obtained for each of the two methods, and their results are then analyzed and compared, both with other series and with the theoretical and simulation results.

It is concluded that the impedance-source inverter topologies offer many advantages over the existing traditional inverters, and can become a very promising converter solution for PV power systems, by increasing their efficiency and granting them the ability to boost their output voltage without requiring an intermediate DC-to-DC converter.

Chapter 1

Introduction

In recent years, the concern for a sustainable and reliable energy system has become increasingly prominent, and the use of renewable energy to relieve this energy problem is becoming important and necessary. A large introduction of renewable power generation in the electrical grid poses a number of issues to the stability and manageability of the whole system. Renewable energy production often requires a wide usage of power electronics converters to achieve the required electrical conversions for grid integration and efficiency optimization.

1.1 Photovoltaic Power Systems

Photovoltaic (PV) power systems, are able to convert the solar irradiation into electricity. Generally, they can be divided into standalone systems and grid-connected systems. The direct current (DC) generated by solar panels must be converted to alternating current (AC) for grid injection and common consumer usage. The solution implemented in most cases to obtain the desired AC signal consists of a DC to DC converter coupled with a DC to AC converter. In practical applications, a single-stage configuration, i.e., only a DC to AC inverter, is adopted to ensure the conversion efficiency. In this manner, the output signal of the PV generation system can achieve the designed voltage amplitude and frequency, while also being able to use a maximum power point tracking (MPPT) algorithm to obtain the maximum possible power from the solar panels.

In the case of a two-stage conversion system, the DC to DC converter is essentially tasked with two roles: converting its input to a voltage level suitable for adequate operation of its coupled power inverter, and forcing the solar panel arrays to produce the maximum possible power under varying conditions. Meanwhile, the DC to AC inverter is tasked with converting its DC input signal, from the DC

to DC converter output, into a desired AC signal in terms of amplitude, frequency, and phase.

The MPPT algorithm is usually implemented by controlling the duty cycle of the DC to DC converter in a closed loop. Meanwhile, the AC voltage level is controlled by regulating the amplitude modulation index of the power inverter.

In conclusion, there are three main components in most PV systems:

- Solar panels, which absorb and convert sunlight into electricity.
- A solar controller (a DC-DC converter) to provide the electrical storage with the best charging current and voltage to quickly, smoothly and efficiently charge it, and extend its service life as much as possible. Another purpose of most commercially available solar controllers is to ensure that the maximum amount of electrical power is generated at all times, by implementing MPPT techniques.
- A solar inverter to change the electric current from DC to AC, to make it suitable for grid and common appliance standards.

As the inverter is an important part of PV systems, the study of inverters is essential for improving their efficiency and reliability.

1.2 Traditional Converter Topologies

There are two types of DC to AC and AC to DC converters: current-source and voltage-source, often also called current-fed and voltage-fed, respectively, and abbreviated as I-source and V-source. Basic schematics for the three-phase variants of both the voltage-source and the current-source inverters are shown in Figure 1.1 and 1.2, respectively. The most commonly used power converter type is the voltage-source converter. This type of converter has, however, several conceptual limitations:

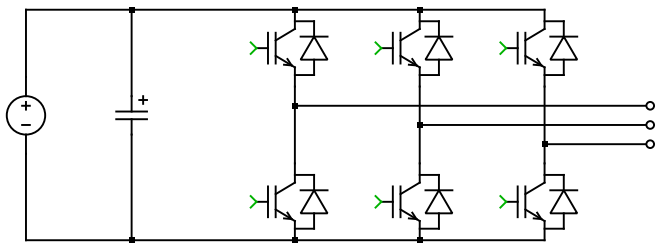


Figure 1.1: Traditional voltage-source three-phase inverter.

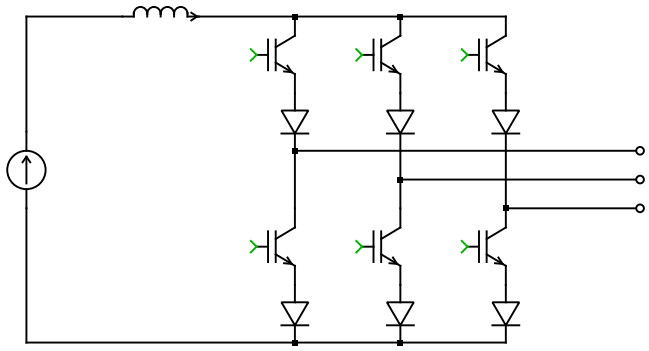


Figure 1.2: Traditional current-source three-phase inverter.

- The V-source inverter cannot achieve an AC output voltage higher than the input voltage, while the V-source rectifier can only achieve higher DC output voltage than the input. The V-source converter is then a buck inverter and boost rectifier.
- The switching devices of each leg of the converter cannot be gated on simultaneously, in order to avoid short-circuiting the power source and damaging the switching devices.
- An output filter is required to achieve a sinusoidal output voltage. This filter is commonly based on inductors and capacitors, such as the LC filter. Other types of high-order filters, such as the LCL filter, are also common.

The I-source converter also has several limitations:

- The AC output voltage has to be greater than the DC input, when operating as an inverter. Therefore, compared to the V-source converter, the I-source converter is always a boost inverter and a buck rectifier.
- At least one leg of the converter has to have all its switching devices gated on at all times. Otherwise, an open circuit of the DC inductor would occur and potentially destroy the power source, while also damaging the switching devices.
- The main switches of the I-source converter have to block reverse voltage, requiring the use of series diodes and limiting the types of adequate switching devices.

Both types of converters also present a series of common core issues, which can be summarized as such:

- They are either a boost or a buck converter, limiting the ranges of the voltage they can operate with.
- Their main circuits cannot be interchangeable. Therefore, a V-source converter main circuit cannot be used for the I-source converter, nor vice versa.
- Both converters are vulnerable to electromagnetic interference (EMI) noise in terms of reliability, due to the limitations imposed by each topology on the switching devices of their inverter legs.

1.3 Impedance-Source Converters

In order to overcome the limitations of the V-source and I-source power converters, a topology was presented by F. Z. Peng in 2003. The paper introduces an impedance-source power converter structure (also referred to as a Z-source converter), which uses an impedance network to couple the converter main circuit to the power source. In this first form, the impedance network is constituted by two inductors connected in series between both terminals of the power source and their respective converter terminals, and two capacitors connected in parallel across the opposite ends of the inductors, as shown in Figure 1.3.

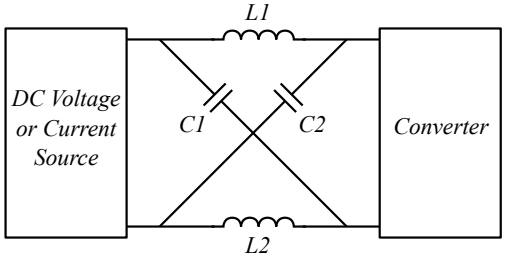


Figure 1.3: Impedance-source network proposed by F. Z. Peng [8].

The impedance network consists of a coupled inductor L_1 and L_2 and capacitors C_1 and C_2 connected in the shown X shape. In Figure 1.3, two separate inductors are adopted. The inductances L_1 and L_2 can be provided through either two separate inductors or a coupled inductor. The impedance source between the power source and the converter allows the DC source or load to be either voltage or current based, adding more flexibility to the sources and loads that can be employed with the converter.

The impedance-source concept can be applied to all types of power conversion: DC-to-DC, AC-to-AC, AC-to-DC, and DC-to-AC. The focus of this paper is on the DC-to-AC impedance source power converter, i.e., the Z-source inverter. The equivalent circuit of such a converter is shown in Figure 1.4. In the case of a current-fed impedance-source inverter, the same structure can be utilized, with the

only modification of connecting the diode in parallel with the power source, as shown in Figure 1.5.

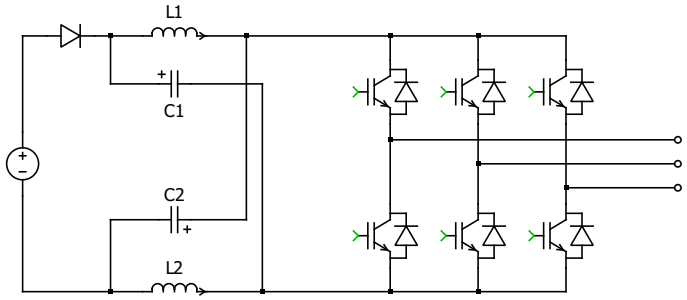


Figure 1.4: Voltage-fed impedance-source inverter as proposed by F. Z. Peng.

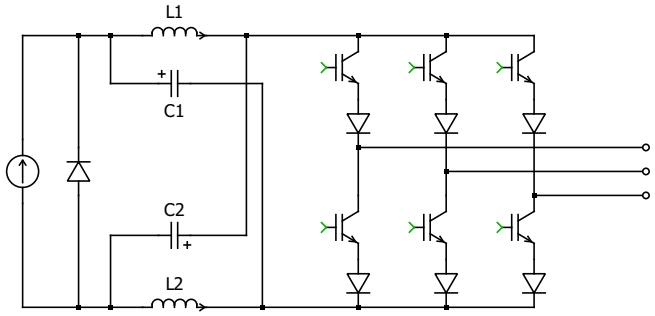


Figure 1.5: Current-fed basic impedance-source inverter as proposed by F. Z. Peng.

Operating principle

The most unique feature that the Z-source inverter provides with respect to conventional V-source and I-source inverters is its ability to obtain a wide range of output AC voltages; theoretically being able to obtain any value between 0 and infinite output voltage regardless of the input voltage. Therefore, the Z-source inverter can operate as a buck-boost inverter.

The Z-source inverter has one more permissible switching state than the traditional V-source inverter. The latter has a total of 8 permissible switching states (vectors), referring to a conventional 3-phase inverter. This corresponds to the 6 active states when the DC voltage is applied to the load, plus the two zero states occurring when the load terminals are shorted through either the three upper or the three lower switching devices. The Z-source inverter adds another permissible zero state to these states, which occurs by shorting the load terminals through both the upper and lower switching devices of any phase leg (both are switched gated on). This stage can be generated in seven different ways: three by shorting

any single phase leg, three by the combination of any two phase legs, and the last one by shorting all three legs simultaneously. The third zero state is called the shoot-through zero state, and would be a forbidden state in a conventional Z-source inverter. The Z-source network is what allows this state to be possible, and provides the unique buck-boost feature to the inverter.

In order to incorporate the shoot-through zero states to the traditional PWM inverter control, a modified version of the PWM signals must be used, forcing all the switching devices on any single branch of the inverter to be gated on simultaneously.

During the shoot-through states, the inductors of the impedance network increase their level of stored energy, while the capacitors discharge. During the non-shoot-through states, the capacitors are charged and the inductors are discharged, resulting in an increase of the average DC-link voltage across the inverter legs; and thus allowing the output signal to also be boosted.

1.4 Classification

The Z-source converter has sparked a notably large amount of research interest. Many different topologies and modifications have been proposed for all types of power conversion (DC-to-AC, AC-to-DC, DC-to-DC, AC-to-AC), each with its unique features for use in different applications.

One way of categorizing the different types of Z-source converter topologies is according to their Z-source networks. Several different groups can be formed [7].

- Original impedance-source network, as shown in Figure 1.3.
- Quasi-impedance-source network, as shown in Figure 1.6 coupled with a three-phase inverter. Figure 1.6 shows the basic continuous input current variant of the qZSI, but several modifications to this network have been proposed.
- Transformer-based impedance-source network, as shown in Figure 1.7, again coupled with a three-phase inverter. Several variations to this topology were also reported in the literature, always using two magnetically coupled inductors.
- Other types of impedance-source network, including topologies such as: the embedded Z-source, semi-Z-source, distributed Z-network, switched-inductor Z-source, and tapped-inductor Z-source.

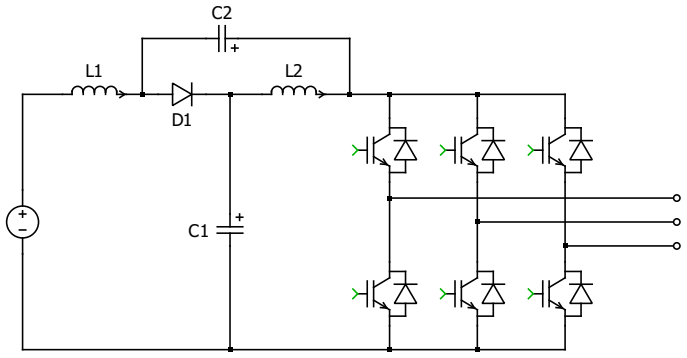


Figure 1.6: Three-phase inverter with quasi-Z-source network [2].

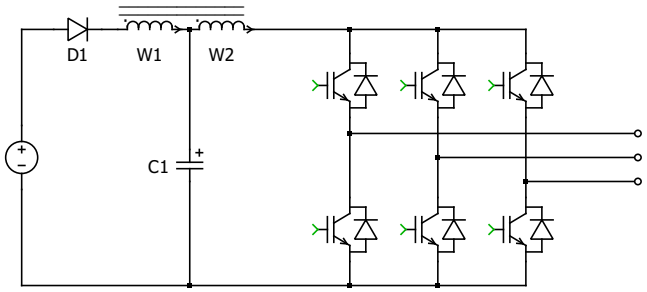


Figure 1.7: Three-phase inverter with trans-Z-source network [6].

The large amount of the reported impedance-source networks are often aimed at fulfilling one of several of these objectives: reduction of the component count and/or rating, increase of the effective voltage boost range, and optimization for concrete applications [6].

Four quasi-Z-source inverter topologies were first proposed by Anderson and Peng in 2008 [2]. These topologies aimed to mitigate some of the problems of the original impedance-source inverter. Namely, they require lower-rating passive components, input current, and provide a common negative DC rail between the power source and the inverter. Among these benefits, the most notable ability of drawing continuous input current makes the quasi-Z-source concept spread to renewable power generation and motor drives.

Another suggested impedance-network topology is the embedded-Z-source network, which is also able to achieve a lower capacitor voltage rating and continuous input current, while also allowing separate connection of multiple sources. Therefore, it may be suitable for PV applications, allowing several generator modules to be connected to the network separately. However, it does not provide a common negative DC rail, since a series inductor is required for each source.

The original Z-source, quasi-Z-source, and embedded-Z-source all share the capability of being able to achieve a theoretically unlimited output voltage gain. However, the higher the voltage gain is, the more voltage stress the inverter switches will receive. Trans-Z-source networks were then proposed to achieve higher voltage gains while keeping voltage stress low. They also reduce component count to a single transformer or coupled inductor and a single capacitor, as shown in Figure 1.7. Several other impedance networks have been proposed to achieve higher voltage gain ranges by adding more components to the network, becoming even higher order impedance network.

1.5 Quasi-Z-Source Inverters

The main advantages for the Z-source inverter can be summarized as:

- Higher reliability than the conventional voltage source inverters, i.e., allowing shoot-through states (short circuits) without damaging any components.
- Ability to boost the DC-link voltage with shoot-through states.

Another topology that aims to further improve the characteristics presented by the Z-source inverter is the quasi-Z-source inverter (qZSI). There are two types of voltage-fed quasi-Z-source inverter:

- The qZSI draws a continuous constant DC current from the DC source. As it is shown in Figure 1.6, it adopts an asymmetrical structure. By adjusting the position of the inductor L_2, it is connected in series with the DC power supply, so that the input current of the Z-source inverter is continuous, which effectively simplifies the filter circuit and reduces the system volume and cost. Therefore, the input stress received of the qZSI will be notably lower, being especially suitable for PV applications.
- The qZSI variant that further decreases the capacitor voltage stress. As it is shown in Figure 1.8, it adjusts the position of the cathode node of the capacitor C_1 based on Figure 1.6, so that the capacitor voltage is consistent with the power supply, thereby greatly reducing the voltage stress across the capacitor.

Compared to the ZSI, the qZSI can then lower the capacitance rating of C_2, since it is not required to sustain such a high voltage. By reducing the input stress, the capacitance for the output of the PV panels can also be reduced, although practically, this capacitance is usually small. Moreover, the qZSI uses a common DC rail between the source and the inverter, which is easier to assemble, and thus it causes less issues with electromagnetic interference.

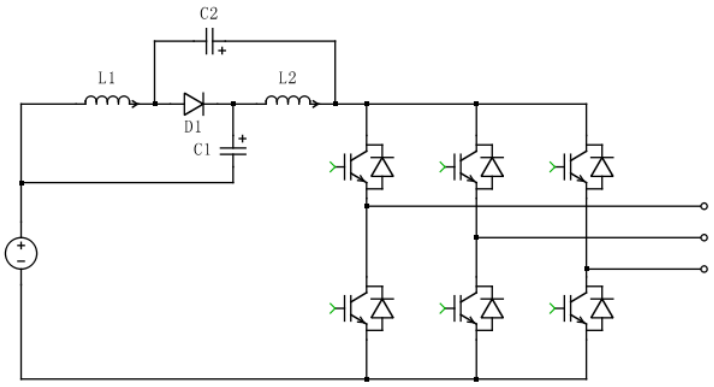


Figure 1.8: Quasi-Z source inverter with reduced capacitor voltage stress.

1.6 Problem Statement

The most commonly used inverter topology in PV power systems is the voltage-source inverter. This type of inverter has the main disadvantage of not being able to boost the input voltage, as previously discussed; as such, it always operates as a buck or step-down inverter. Assuming a simple PWM control, the output voltage is related to the input voltage by the amplitude modulation ratio as:

$$V_{out} = MV_{in}, \quad M = \frac{V_{sine}}{V_{tri}} \tag{1.1}$$

where V_{sine} and V_{tri} are the sinusoidal and triangular reference signals, respectively, for the PWM signal generation; and M is the amplitude modulation index. For most applications, the amplitude modulation index is kept at or below 1. Increasing it above this value by making the amplitude of the sinusoidal signal larger than that of the triangular signal makes the system overmodulated, notably increasing the harmonic content of the output waveform. Therefore, voltage-source inverters for PV applications most often operate with a step-up DC-to-DC converter in order to reach the desired voltage level. This, however, increases component count and reduces the entire system efficiency.

As stated earlier in this chapter, a way to solve this and other issues found in conventional inverter topologies is the introduction of an impedance-source network between the power source and the inverter bridge. The research question is then formulated - can the performance of PV power systems be improved with the impedance source converters? To answer this question, this project aims to analyze the operating principles of impedance-source inverters and study their possible uses in PV systems. Particularly, its focus is on the analysis of the voltage-fed

quasi-Z-source inverter. Simulation models and experimental tests will be developed for this topology.

Project Limitations

This project is limited to the study of the quasi-Z-source inverter, especially its three-phase variant. The undertaken theoretical analysis of the qZSI will always assume the inverter to be in continuous operation mode, and as such the discontinuous operation mode will only appear in simulations and experimental tests. The analysis will also not consider transient states. The control schemes analyzed will consider open-loop schemes.

Chapter 2

Circuit Analysis and Basic Design

This chapter is aimed to discuss in detail the theoretical basis behind the quasi-Z-source inverter. To do so, the basic steady-state circuit analysis for the three-phase qZSI is provided. The performed analysis is only focused on the DC components of the different parameters of the qZSI, and does not take ripple signals into consideration. As such, it also does not consider the effect of passive component parameters.

2.1 Basic Analysis of the Quasi-Z-Source Inverter

The Z-source network does not require additional switching devices. It only requires the use of the three-phase inverter, which can consist of as few as 6 switching devices. With specifically designed control methods, the boost function can be safely performed. In addition, from the inverter side it is a voltage-fed inverter, so it also has buck function compared to the bus voltage, by controlling the modulation index of the gating signals. So the qZSI can achieve the functions of boosting and bucking, as it will be proven in the following section by analyzing the circuit of the qZSI.

The qZSI has two working states: the shoot-through state and the non-shoot-through state [6]. The shoot-through state occurs when one or several of the inverter legs are shortcircuited, whereas non-shoot-through states designate the whole set of allowed states in a traditional voltage-source inverter.

When the circuit is in shoot-through state, the Z-source network inductor charges and the capacitor discharges. When the circuit is at a non-shoot-through state, the Z-source network inductor discharges, the capacitor is charged, and the diode is forwarded. The equivalent circuits of two states are shown in the Figure 2.1, (1)

and (2), respectively.

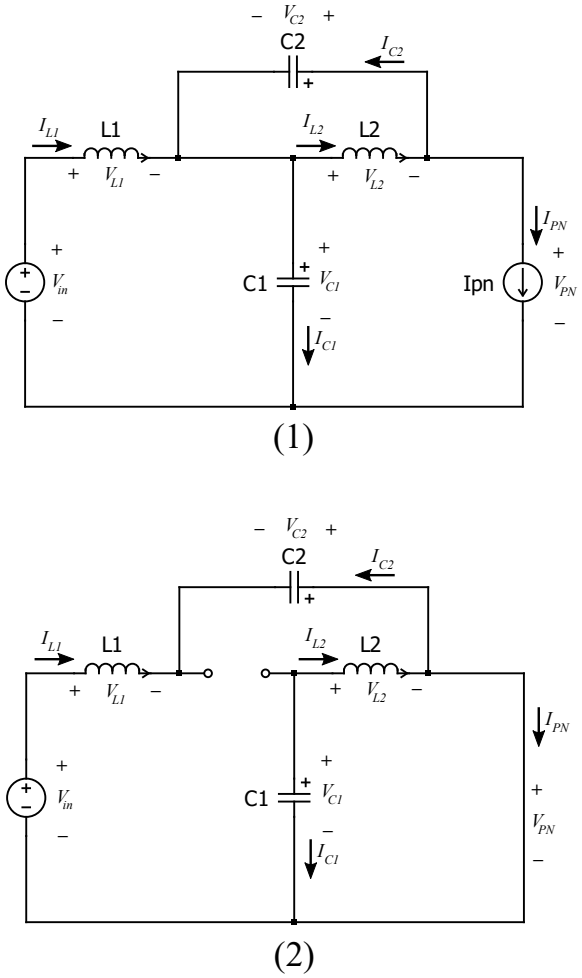


Figure 2.1: Equivalent circuit of the qZSI in (1) non-shoot-through state, and (2) shoot-through state.

All voltages and currents present in the circuit are defined in Figure 2.1. Assuming one switching cycle lasts for a time interval T_s, the interval of the shoot-through lasts for T_{sh} in each switching cycle, and the non-shoot-through time interval is T_{nsh}. Thus, $T_s = T_{sh} + T_{nsh}$, and the shoot-through duty ratio can be defined as $D = T_{sh}/T_s$.

From Figure 2.1 (1), the following can be obtained:

$$v_{L1} = V_{in} - V_{C1} \qquad v_{L2} = -V_{C2} \tag{2.1}$$

$$v_{PN} = V_{C1} - v_{L2} = V_{C1} + V_{C2} \qquad V_{diode} = 0 \tag{2.2}$$

From Figure 2.1 (2), another set of equations can be:

$$v_{L1} = V_{C2} + V_{in} \qquad v_{L2} = V_{C1} \tag{2.3}$$

$$v_{PN} = 0 \qquad v_{diode} = -(V_{C1} + V_{C2}) \tag{2.4}$$

During one switching cycle, assuming a steady-state operation, the average voltage over the inductors is zero. Therefore:

$$V_{L1} = \frac{T_{sh}(V_{C2} + V_{in}) + T_{nsh}(V_{in} - V_{C1})}{T_s} = 0$$

$$V_{L2} = \frac{T_{sh}(V_{C1}) + T_{nsh}(-V_{C2})}{T_s} = 0$$

leading to

$$V_{C1} = \frac{(1-D)V_{in}}{1-2D} \qquad V_{C2} = \frac{DV_{in}}{1-2D} \tag{2.5}$$

From equations 2.1, 2.3, and 2.4, the peak DC-link voltage across the inverter bridge can be derived as:

$$V_{PN} = V_{C1} + V_{C2} = \frac{V_{in}}{1-2D} = BV_{in} \tag{2.6}$$

where B is the boost factor of the qZSI, and $B \geq 1$. Theoretically, B ranges from 1 when the shoot-through ratio is 0, resulting in the inverter not boosting voltage, to infinite boost factor when the shoot-through duty ratio is 0.5. This relationship is illustrated in Figure 2.2.

Therefore, the AC peak phase voltage V_{ac} and voltage gain G are defined as:

$$V_{ac} = \frac{MBV_{in}}{2} \tag{2.7}$$

$$G = BM \tag{2.8}$$

where M is the modulation index.

By using the system power rating P, the average current of the inductors L_1, L_2 can be deduced as:

$$I_{L1} = I_{L2} = I_{in} = P/V_{in} \tag{2.9}$$

According to the Kirchhoff's current law and equation 2.9, the follwing can be obatained:

$$I_{C1} = I_{C2} = I_{PN} - I_{L1} \qquad I_D = 2I_{L1} - I_{PN} \tag{2.10}$$

From equation 2.8, it can be deduced that the qZSI can both buck and boost the voltage by modifying the boost factor B, proportional to the shoot-through duty ratio D, and the modulation index M.

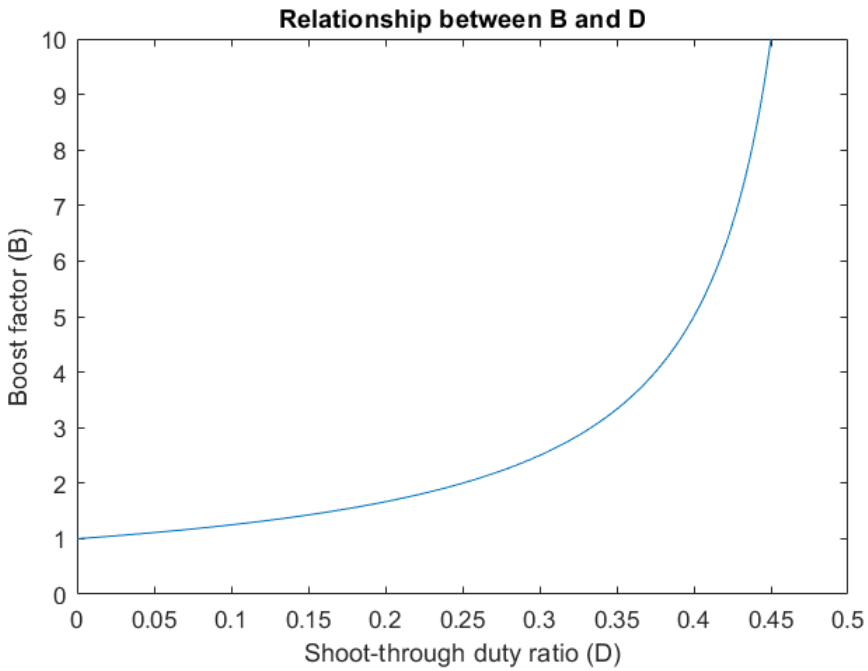


Figure 2.2: Relationship between the boost factor and shoot-through duty ratio of the qZSI.

2.2 Analysis of the Three-Phase qZSI

This section is intended to provide the basic guidelines for the design of the passive components of the impedance source parameters. It includes the necessary circuit analysis to obtain the expressions for the ripple signals. From these equations, the expressions for the minimum requirements of the passive components are obtained. This analysis will be performed for both the three-phase quasi-Z-source inverter and, afterwards, the more complicated single-phase quasi-Z-source inverter.

Inductors and capacitors are the main components that distinguish the qZSI from a traditional inverter, so it is fundamental to appropriately design the right parameters of inductance and capacitance in order to guarantee the correct functioning of the qZSI. For three-phase qZSI, the impedance design of qZSI network should limit the switching frequency current and voltage ripple. However, the situation is more complicated for single-phase inverters, the 2ω ripple that appears in the signals of such a setup must also be taken into consideration, as it significantly increases inductance and capacitance requirements.

Inductance

For the inductors, inductance and over-current values should be taken into consideration [6]. On the one hand, if the inductance is too low for the desired operation of the inverter, it will cause the current to become discontinuous, i.e., by having its ripple hit the zero current, increasing the complexity of the system control, inductor heat loss, and thereby also cooling requirements. When the inductance of the Z-source inductor is too small, it will have a weak inhibitory effect on the current flowing through it. The current of the inverter flowing through the switching devices at shoot-through will rise sharply, which can result in the component destruction.

On the other hand, using too large an inductor can unnecessarily increase system cost, together with increasing the resistive component of the inductor. As observed in simulations, it can also lengthen the transient states of the inverter operation. Therefore, once the designed inductor meets the requirements that guarantee the stability of the inverter system, the value of the Z-source inductance should be minimized.

According to the analysis in Chapter 2, during the shoot-through state the following relationship is valid [1]:

$$\delta i_{L1} = \delta i_{L2} = \delta i_L = \frac{V_L}{L} \times \delta T = \frac{DV_{in}}{(1-2D)L} \times \delta T \tag{2.11}$$

where V_L is the DC component of the voltage across the inductor, and δT is the shoot-through time. Assuming the inverter to operate with simple boost control, then $\delta T = DT_s/2$. Therefore, the inductance should meet the requirement:

$$L_1 = L_2 \geq \frac{D^2 V_{in} T_s}{2(1-2D)\delta i_{L,max}} \tag{2.12}$$

Capacitance

For the design of capacitors, the capacitance and maximum voltage rating are the main aspects that should be considered. According to the discussions in Section 2, we know that the voltage across the capacitors can be expressed as:

$$V_{C1} = \frac{1-D}{1-2D} \times V_{in}, V_{C2} = \frac{D}{1-2D} \times V_{in} \tag{2.13}$$

So the maximum voltage rating of the capacitors should be equal to or larger than the results in equation 2.13.

For the capacitance, on the one hand, in the Z-source inverter system, the larger its value is, the smaller the voltage ripple of the Z-source capacitor will be, the

higher the stability of the system will be, and the stronger its filtering capability will be. According to these metrics, the value of the capacitance should be as large as possible. On the other hand, the larger the capacitance is, the higher the capacitor costs and power losses will become. As for inductors, the larger the capacitance rating is, the more volume that the capacitors will occupy. Too large a capacitance can also lengthen the transient states of the inverter.

According to the previously presented circuit analysis, during the shoot-through state the current of capacitors is $-i_{L1}$. With a large Z-source capacitance and high switching frequency of the inverter bridge, the voltage ripple of the capacitors becomes smaller. Assuming it is operated with the simple boost control, $\delta T = DT_s/2$, and therefore:

$$\delta v_{C1} + \delta v_{C2} = 2\delta v_C = \frac{I_C}{C} \times \delta T = \frac{I_L D T_s}{2C} \tag{2.14}$$

where I_L is the DC component of inductor current. Thus, the designed capacitance values should meet the requirement:

$$C_1 = C_2 \geq \frac{I_L D T_s}{4\delta v_{C,max}} \tag{2.15}$$

2.3 Analysis of the Single-Phase qZSI

Although most of this report is focused on the three-phase qZSI, it is also common to utilize the single-phase qZSI as shown in Figure 2.3. In the non-shoot-through state, the qZSI transfers the power from the DC side to the AC side, while there is no power transmission in the shoot-through state. If there is no power loss i.e., assuming an ideal circuit-, there is a power balance, resulting in [12], [6]:

$$v_{PN} \times i_{PN} \times ((1 - D) + 0 \times D) = v_{ac} \times i_{ac} \tag{2.16}$$

where v_{PN} consists of the voltage value at the DC side plus the 2ω ripple component, i_{PN} represents the current entering into the inverter bridge averaged over the switching period, D is the shoot-through duty ratio, and v_{ac} and i_{ac} are the output voltage and current at the AC side, respectively.

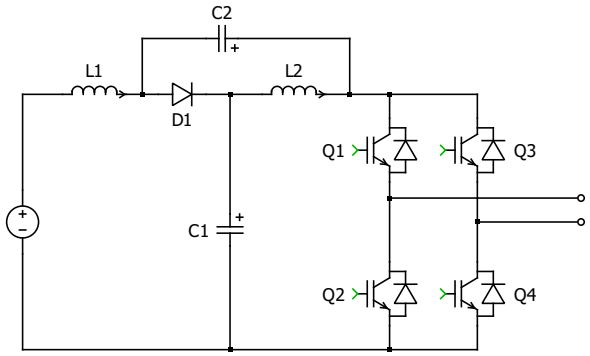


Figure 2.3: Single-phase qZSI inverter.

Assuming the voltage and current output of the qZSI to be $v_{ac} = V_{ac} \times \sin(\omega t)$, and $i_{ac} = I_{ac} \times \sin(\omega t - \phi)$ respectively, respectively, where ω is the angular frequency, ϕ is the impedance angle, and V_{ac} and I_{ac} are the amplitudes of the AC output voltage and current, respectively.

The voltage at the DC side and AC side follows the relationship:

$$v_{ac} = m \times v_{PN} \tag{2.17}$$

where $m = M \times \sin \omega t$, and M is the modulation index.

From equations 2.16 and 2.17, and using the trigonometric identity $\sin(a)\sin(b) = \frac{1}{2}((\cos(a-b) - \cos(a+b))$; i_{PN} can be deduced as:

$$i_{PN} = \frac{MI_{\mathrm{a}}}{2(1-D)}(cos\phi - cos(2\omega t - \phi)) \tag{2.18}$$

which consists of two parts:

- A DC component: $I_{PN} = \dfrac{MI_{\mathrm{ac}}}{2(1-D)} \cos\phi$
- A 2ω component: $\tilde{i}_{PN} = -\dfrac{MI_{ac}}{2(1-D)} \cos(2\omega t - \phi)$

Assuming $L_1 = L_2 = L$, $C_1 = C_2 = C$, and because both i_{PN} and $\tilde{i}_{PN}$ influence the voltage of C_1 and C_2 and the current of L_1 and L_2, they also consist of DC and 2ω components:

$$i_{L1} = I_{L1} + \tilde{i}_{L1} \qquad i_{L2} = I_{L2} + \tilde{i}_{L2}$$
$$v_{C1} = V_{C1} + \tilde{v}_{C1} \qquad v_{C2} = V_{C2} + \tilde{v}_{C2}$$

DC Component

From the discussions in Section 2, and assuming zero voltage drop at the diode, the average capacitor voltages V_{C1}, V_{C2}, and average inductor currents I_{L1} and I_{L2} can be expressed as:

$$\begin{cases} V_{C1} = \dfrac{1-D}{1-2D} V_{in} \\ V_{C2} = \dfrac{D}{1-2D} V_{in} \\ I_{L1} = I_{L2} = I_{in} = \dfrac{P}{V_{in}} = \dfrac{V_{ac} I_{ac} \cos\phi}{V_{in}} \end{cases} \tag{2.19}$$

Since $V_{ac} = \dfrac{M}{1-2D} \times \dfrac{V_{in}}{2}$, we can get: $I_{L1} = I_{L2} = \dfrac{M I_{ac}}{2(1-2D)} \cos\phi$.

2ω Component

According to Section 2, the real components v_{C1}, v_{C2}, i_{L1} and i_{L2} can be expressed as:

In non-shoot-through state:

$$\begin{aligned} v_{L1} &= V_{in} - v_{C1} \\ v_{L2} &= -v_{C2} \\ i_{C1} &= i_{C2} = i_{L1} - i_{PN} = i_{L2} - i_{PN} \end{aligned}$$

In shoot-through state:

$$\begin{aligned} v_{L1} &= V_{in} + v_{C2} \\ v_{L2} &= v_{C1} \\ i_{C1} &= i_{C2} = -i_{L1} = -i_{L2} \end{aligned}$$

In steady-state, assuming V_{in} is constant, there is no 2ω component of V_{in}, so we can get:

In non-shoot-through state:

$$\begin{cases} L_1 \dfrac{d\tilde{i}_{L1}}{dt} = -\tilde{v}_{C1} \\ L_2 \dfrac{d\tilde{i}_{L2}}{dt} = -\tilde{v}_{C2} \\ C_1 \dfrac{d\tilde{v}_{C1}}{dt} = C_2 \dfrac{d\tilde{v}_{C2}}{dt} = \tilde{i}_{L1} - \tilde{i}_{PN} = \tilde{i}_{L2} - \tilde{i}_{PN} \end{cases} \tag{2.20}$$

In shoot-through state:

$$\begin{cases} L_1 \dfrac{d\tilde{i}_{L1}}{dt} = \tilde{v}_{C2} \\ L_2 \dfrac{d\tilde{i}_{L2}}{dt} = \tilde{v}_{C1} \\ C_1 \dfrac{d\tilde{v}_{C1}}{dt} = C_2 \dfrac{d\tilde{v}_{C2}}{dt} = -\tilde{i}_{L1} = -\tilde{i}_{L2} \end{cases} \tag{2.21}$$

As mentioned before: $L_1 = L_2 = L$, $C_1 = C_2 = C$. Therefore, from 2.20 and 2.21, one can find that $\tilde{v}_{C1} = \tilde{v}_{C2}$. The average voltage of the 2ω components of the capacitors and inductors per switching cycle is:

$$\begin{cases} L\dfrac{d(\tilde{i}_{L1})_T}{dt} = L\dfrac{d(\tilde{i}_{L2})_T}{dt} = (1-D)(-\tilde{v}_{C1}) + D\tilde{v}_{C1} = (2D-1)\tilde{v}_{C1} \\ C\dfrac{d(\tilde{v}_{C1})_T}{dt} = C\dfrac{d(\tilde{v}_{C2})_T}{dt} = (1-D)(\tilde{i}_{L1} - \tilde{i}_{PN}) + D(-\tilde{i}_{L1}) \\ \qquad\qquad\qquad\qquad = (1-2D)\tilde{i}_{L1} - (1-D)\tilde{i}_{PN} \end{cases} \tag{2.22}$$

Then, $\tilde{i}_{PN}$ can be deduced as:

$$\tilde{i}_{\mathrm{PN}} = \frac{1}{1-D}\left((1-2D)\tilde{i}_{\mathrm{L1}} - C\frac{d(\tilde{v}_{\mathrm{C1}})_T}{dt}\right) \tag{2.23}$$

Assuming $D < 0.5$, the relationship between these phasors can be obtained according to equations 2.22 and 2.23, as shown in Figure 2.4.

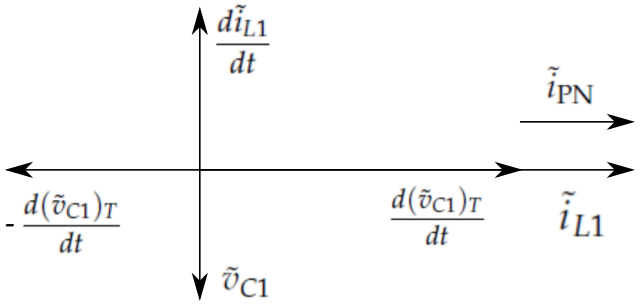


Figure 2.4: Phasor diagram.

Since $\dfrac{d(\tilde{v}_{C1})_T}{dt}$ and $\tilde{i}_{L1}$ have the same phase, $\tilde{i}_{PN}$ also has the same phase as $\tilde{i}_{L1}$.

Then, we can define:

$$\begin{aligned}
\tilde{i}_{L1} &= \hat{i}_{L1}\cos(2\omega t-\phi)\\
\tilde{i}_{L2} &= \hat{i}_{L2}\cos(2\omega t-\phi)\\
\tilde{v}_{C1} &= \hat{v}_{C1}\cos(2\omega t-\phi-\frac{\pi}{2}) = \hat{v}_{C1}\sin(2\omega t-\phi)\\
\tilde{v}_{C2} &= \hat{v}_{C2}\cos(2\omega t-\phi-\frac{\pi}{2}) = \hat{v}_{C2}\sin(2\omega t-\phi)
\end{aligned}$$

where $\hat{i_{L1}}$, $\hat{i_{L2}}$, $\hat{v_{C1}}$, and $\hat{v_{C2}}$ represent the average value of their respective current or voltage ripple signals. Combining these equations with 2.18 and 2.22, one can obtain the following expressions:

$$\begin{cases}
\tilde{i}_{L1} = \tilde{i}_{L2} = \dfrac{(1-2D)}{4LC\omega^2-(1-2D)^2}\times\dfrac{MI_{ac}}{2}cos(2\omega t-\phi)\\
\tilde{v}_{C1} = \tilde{v}_{C2} = \dfrac{2\omega L}{4LC\omega^2-(1-2D)^2}\times\dfrac{MI_{ac}}{2}sin(2\omega t-\phi)
\end{cases} \tag{2.24}$$

Complete model

From 2.19 and 2.25, we can get the complete model of the qZSI inverter, combining both the DC and AC (i.e., the average and ripple) components of each of the main system parameters:

$$\begin{cases}
i_{L1} = i_{L2} = I_{L1} + \tilde{i}_{L1} = \dfrac{1}{(1-2D)}\times\dfrac{MI_{ac}}{2}\cos\phi \\
\qquad\qquad + \dfrac{(1-2D)}{4LC\omega^2-(1-2D)^2}\times\dfrac{MI_{ac}}{2}\cos(2\omega t-\phi)\\
v_{C1} = V_{C1} + \tilde{v}_{C1} = \dfrac{1-D}{1-2D}\times V_{in} \\
\qquad\qquad + \dfrac{2\omega L}{4LC\omega^2-(1-2D)^2}\times\dfrac{MI_{ac}}{2}\sin(2\omega t-\phi)\\
v_{C2} = V_{C2} + \tilde{v}_{C2} = \dfrac{D}{1-2D}\times V_{in} \\
\qquad\qquad + \dfrac{2\omega L}{4LC\omega^2-(1-2D)^2}\times\dfrac{MI_{ac}}{2}\sin(2\omega t-\phi)
\end{cases} \tag{2.25}$$

Therefore:

$$\begin{aligned}
v_{PN} = V_{C1} + V_{C2} = &\frac{1}{1-2D}\times V_{in}\\
&+\frac{2\omega LMI_{ac}}{4LC\omega^2-(1-2D)^2}\sin(2\omega t-\phi)
\end{aligned} \tag{2.26}$$

which also consists of the DC component $V_{PN} = \dfrac{1}{1-2D} \times V_{in}$ and the 2ω component $\tilde{v}_{PN} = \dfrac{2\omega LMI_a c}{4LC\omega^2 - (1-2D)^2} \sin(2\omega t - \phi)$.

Then, the peak-to-peak ripple ratio of the DC-link voltage envelope is:

$$\begin{aligned} a &= \frac{2\hat{v}_{PN}}{V_{PN}} \\ &= \frac{(4\omega LMI_{ac}(1-2D)}{(4LC\omega^2 - (1-2D)^2)V_{in}} \end{aligned} \tag{2.27}$$

where $\hat{v}_{PN}$ is the amplitude of the 2ω voltage component.

From equations 2.19 and 2.25, one can find that the 2ω current ripple ratio of inductor is:

$$\begin{aligned} b &= \frac{\hat{i}_{L1}}{I_{L1}} \\ &= \frac{(1-2D)^2}{4LC\omega^2 - (1-2D)^2 \cos\phi} \end{aligned} \tag{2.28}$$

where $\hat{i}_{L1}$ is the amplitude of the 2ω current component.

Then, assuming the allowed maximum voltage ripple and current ripple ratios to be a^* and b^*, respectively, the capacitance and inductance of the impedance network should meet the following requirements:

$$C \geq \frac{(1-2D)(1+b^*\cos\phi)MI_{ac}}{a^*\omega V_{DC}} \tag{2.29}$$

$$L \geq \frac{a^* V_{DC}(1-2D)}{4\omega b^* MI_{ac}\cos\phi} \tag{2.30}$$

Taking as an example the following data group: $D = 0.2$, $M = 0.6$, $\omega = 314$ rad/s, $\cos\phi = 0.9948$, $I_{ac} = 0.5$ A, and $V_{DC} = 30$ V; we can graph Figures 2.5 and 2.6, according to (2.27) and (2.28).

As expected, Figures 2.5 and 2.6 show that the 2ω ripple of the DC-link voltage envelope decreases significantly when the capacitance increases and it decreases slowly when the inductance increases. However, the 2ω ripple of the inductor current decreases significantly with both of capacitance and inductance increasing.

Equations 2.27 and 2.28 show that the larger the shoot-through duty ratio D is, the lower the requirements for both capacitance and inductance of the Z-source network will be. Both requirements also decrease when the output frequency ω is increased. However, the capacitance requirement is directly proportional to the

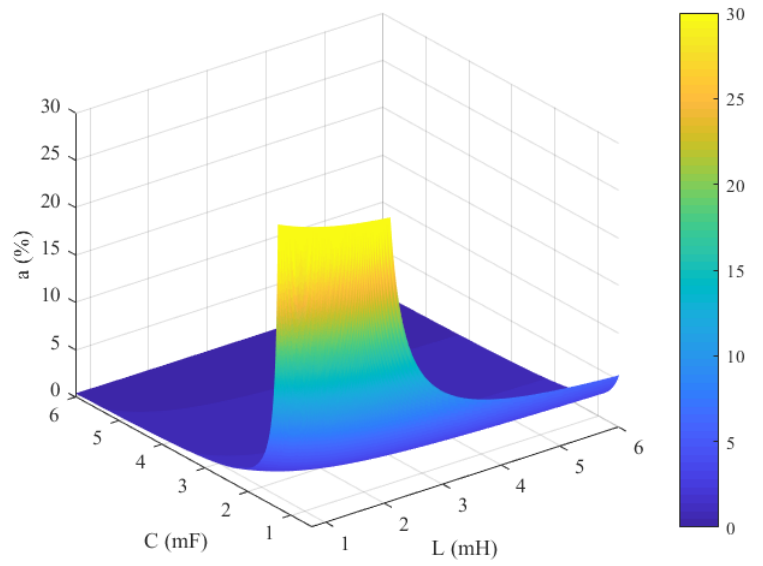


Figure 2.5: 2ω ripple ratio of the DC-link voltage envelope.

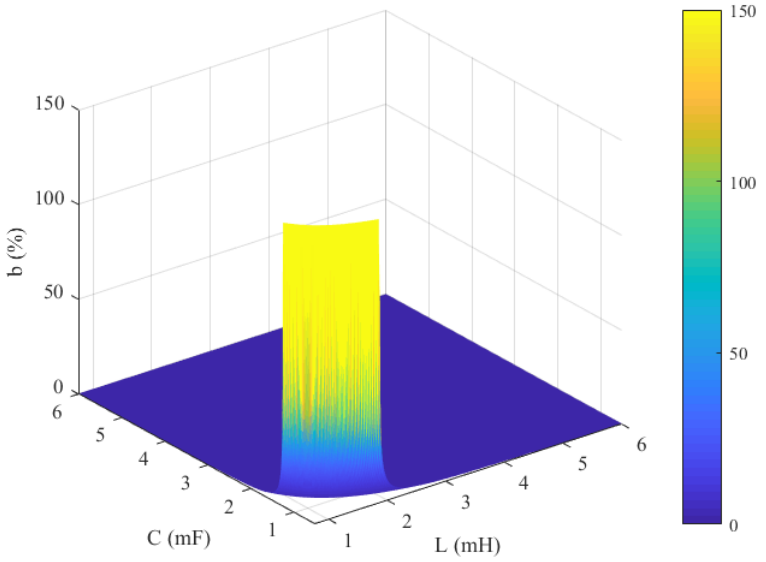


Figure 2.6: 2ω ripple ratio of the inductor current.

modulation index M, the output current I_{ac}, the load power factor $\cos\phi$, and the allowed 2ω ripple ratio of the inductor current b^*; whereas the inductance requirement is inversely proportional to these parameters. On the other hand, the capac-

itance requirement is inversely proportional to the DC input voltage V_{DC} and the allowed 2ω ripple ratio of the DC-link voltage envelope a^*; while the inductance requirement is directly proportional to both parameters.

2.4 Summary

For the circuit analysis part of this chapter, the most important result is the output sinusoidal voltage obtained by the qZSI. This result is defined by the following equation:

$$V_{out} = \frac{V_{PN} \times M}{2}$$

where V_{PN} is the DC-link voltage, defined as:

$$V_{PN} = B \times V_{in}$$

B is the boost factor, derived from the shoot-through duty ratio as:

$$B = \frac{1}{1-2D}$$

This expression always holds for the qZSI when operating in continuous mode.

For the design of the qZSI passive components, the most important results are the inductance and capacitance requirements, together with the current through the inductors and the voltage stress of capacitors. These parameters can be calculated as:

$$L_1 = L_2 = \frac{D^2 \cdot V_{in} \cdot T_s}{2(1-2D)\delta i_{L,max}} \qquad C_1 = C_2 = \frac{I_L \cdot D \cdot T_s}{4\delta v_{C,max}}$$

$$I_{L1} = I_{L2} = \frac{P}{V_{in}} \qquad V_{C1} = \frac{1-D}{1-2D} \times V_{in} \qquad V_{C2} = \frac{D}{1-2D} \times V_{in}$$

Chapter 3

Modulation Methods

This chapter focuses on the main modulation methods that can be used to generate the gating signals of the three-phase quasi-Z-source inverter, based on modifications on the modulation methods used for traditional three-phase inverters. *PLECS*-based implementation examples are also included for the different analyzed modulation methods. The different modulation methods are then compared.

3.1 Introduction

An inverter converts the input DC signal into AC, which is mainly achieved by utilizing a certain modulation method to generate the gating signals for the inverter bridge switches. In this section, the focus will be on pulse width modulation (PWM) control methods and their comparison.

The PWM method is presently the most common control method for inverters. This method is based on the use of a constant switching period for each switching device, which is then subdivided in two active and inactive states, the duration (width) of which is controlled in such a way that allows for the desired output result.

The basic idea behind PWM is to obtain a waveform that minimizes low-frequency harmonics, so that they can then be easily filtered out by a low-pass filter, commonly a simple LC filter. Nonetheless, PWM methods can be broadly classified into several different groups, each offering different benefits: sinusoidal i.e. carrier-based pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), specific harmonic elimination pulse width modulation (SHEPWM), Delta pulse width modulation, etc.

3.2 Carrier-Based Pulse Width Modulation

Classic carrier-based, or sinusoidal, PWM is likely the simplest form for a three-phase inverter that allows the inverter output signal to be a high-quality sinusoidal. The gating signals of the switching devices are obtained by comparing three reference sinusoidal signals, each shifted by 120°, to a carrier signal. This carrier signal is often implemented as a sawtooth or triangular wave.

Frequency modulation. Using this method, the output signal harmonic content shows a peak at the frequency of the reference sinusoidal signals, together with harmonic packets at higher frequencies. These harmonics are located at:

$$n = jm_f \pm k \tag{3.1}$$

where $j = 1, 3, 5, ...$ for $k = 2, 4, 6, ...$; and $j = 2, 4, ...$ for $k = 1, 5, 7, ...$, such that n is not a multiple of three. The frequency modulation factor m_f is obtained as the quotient of the triangular/sawtooth carrier signal frequency over the reference sinusoidal frequency [9]. Therefore, these harmonics appear at higher frequencies when the the carrier frequency is higher, assuming constant reference frequency. Therefore, the higher the carrier frequency, the easier it will be for the undesired harmonic packets to be filtered out.

However, the higher the frequency of the carrier wave is, the higher the switching frequency of the switching devices, and thereby the power losses at the switching devices will also be higher. Therefore, there is a compromise between the harmonic content, or filter parameters, and power loss at the switching devices, which forces the design to account for more heat dissipation. This compromise between undesired harmonic content and switching losses is found in most modulation techniques.

Amplitude modulation. The output amplitude of a three-phase inverter with sinusoidal carrier-based PWM is related to its DC input voltage and the amplitude modulation factor M, which is defined as the quotient of the reference sinusoidal amplitude over that of the triangular/sawtooth carrier. The output amplitude of the fundamental AC output phase voltage can be obtained as:

$$\hat{v}_{an1} = M \cdot \frac{V_s}{2} \quad \text{for} \quad 0 < M \leq 1 \tag{3.2}$$

When increasing the amplitude modulation factor above 1 by using sinusoidal references with larger amplitude than the carrier signal, the inverter enters into the overmodulation region. In this region, the phase voltages range in:

$$\frac{V_s}{2} < \hat{v}_{an1} = \hat{v}_{bn1} = \hat{v}_{cn1} < \frac{4}{\pi} \cdot \frac{V_s}{2} \tag{3.3}$$

Therefore, the fundamental voltage can be further increased to up to 0.637 times the DC input voltage. However, using overmodulation to increase the voltage leads to the introduction of undesired harmonics. In order to reach the maximum possible output voltage, the inverter requires full overmodulation, in which case the switching devices are on for 180°and the output waveform is square. When using overmodulation, the phase output voltage contains the harmonics f_m with frequencies, where $m = 6k \pm 1, \quad k = 1, 2, 3, ...$, and their amplitudes are inversely proportional to their harmonic order m. Therefore:

$$\hat{v}_{anm} = \frac{1}{m} \cdot \frac{4}{\pi} \cdot \frac{V_s}{2} \tag{3.4}$$

Other types of the carrier-based pulse width modulation introduce modifications to the basic control scheme in order to achieve different results. Most commonly, they aim to maximize the AC output voltage. This is the case of the 60°-PWM and third-harmonic PWM. The basic idea behind these modified PWM methods is to inject selected harmonics to the output waveform in order to allow the fundamental frequency to increase while keeping the peaks of the sinusoidal output at or below the DC input voltage. This allows for a better utilization of the DC supply voltage than that of the sinusoidal PWM. The presence of the exact same third-harmonic component in each phase results in a cancellation of this component in the neutral terminal. Therefore, the line-to-neutral phase voltages are all sinusoidal. The peak line voltage achieved by both of this methods is $V_L = \sqrt{3} \times 0.577 V_s$, which represents an increase of approximately 15.5% with respect to the standard sinusoidal PWM [9].

Carrier based PWM for Z-source inverters. As stated in this section, one of the most important objectives of the PWM control is achieving the maximum possible utilization of the DC supply voltage. Impedance-source inverters grant a much higher flexibility in this sense, as they are able to operate as buck-boost inverters. When designing control schemes for ZSIs, control methods for standard three-phase inverters are often taken as a basis, and are then modified to account for the introduction of shoot-through states.

There exist three classic carrier-based PWM methods for the ZSI/qZSI: simple boost control (SBC), maximum boost control (MBC), and maximum constant boost control (MCBC). They generate the shoot-through states by applying different shoot-through references to the traditional carrier-based sinusoidal PWM. The major difference between different control methods are the shoot-through reference voltages V_p, and V_n, corresponding to the positive and negative voltage references, respectively. When the carrier, i.e. the triangle wave, is greater than V_p and the upper envelope of three-phase modulating waves (V_a, V_b, V_c) or is lower than V_n and the lower envelope of three-phase modulating waves, the switching devices conduct together, which produces the shoot-through states [6].

3.2.1 Simple Boost Control

In the simple boost control [6], the reference voltages V_p and V_n, where ($V_n = -V_p$), are constant. One is greater or equal to the upper envelope of the modulating waves and the other is lower or equal to the lower envelope of the modulating waves. The simulation circuit and sketch map of the simple boost control are shown in the Figures 3.1 and 3.2 respectively.

In the simple boost control, the shoot-through time per cycle is constant, which means that the boost factor is constant, so the DC inductor current and capacitor voltage have no ripple associated with the output frequency. From Figure 3.2, we can see that shoot-through duty ratio $D = 1 - V_p/V_{tri}$, with a modulation index of $M = V_{sine}/V_{tri}$, where V_{tri} is the amplitude of the triangular wave, and V_{sine} is the amplitude of the sine wave. Because V_p is greater or equal to V_{sin}, the maximum shoot-through duty ratio D_{max} is $(1 - M)$. When M increases to 1, D is 0, at which point the qZSI operates as a normal VSI.

Figure 3.1 shows an example of a possible implementation of the simple boost control in *PLECS*, with the control scheme used in a three-phase quasi-Z-source inverter with an LC output filter.

As seen in Figure 3.1, the implementation of the control scheme for the simple boost does not differ much from that of the conventional sinusoidal PWM. A constant value is taken for the reference voltage V_p, which is then compared with the existing triangular carrier. The same comparison is performed again with the negative reference voltage V_n, obtained by inverting V_p. By adding both of these generated signals together, the shoot-through signal is obtained. This shoot-through signal can then be added to the conventional PWM switching signals, obtaining the modified signals which include the shoot-through states.

It should be noted that the shoot-through signal can be added to the standard switching signal in different ways. In Figure 3.1, the shoot-through signal is included in all 6 switching devices, so that all three legs of the inverter are short-circuited at the same time. The inverter can also be short-circuited by introducing the shoot-through signal in any single leg or any combination of two legs. However, by gating on all switching devices simultaneously their total voltage stress is reduced. Therefore, it is often preferable to use all three legs simultaneously to introduce the shoot-through states.

3.2.2 Maximum Boost Control

In the maximum boost control, the reference voltages V_p and Vn are the upper and lower envelope of the modulation waves. The simulation circuit (only the part of PWM generator, the main circuit is the same as that of Figure 3.1) and sketch map

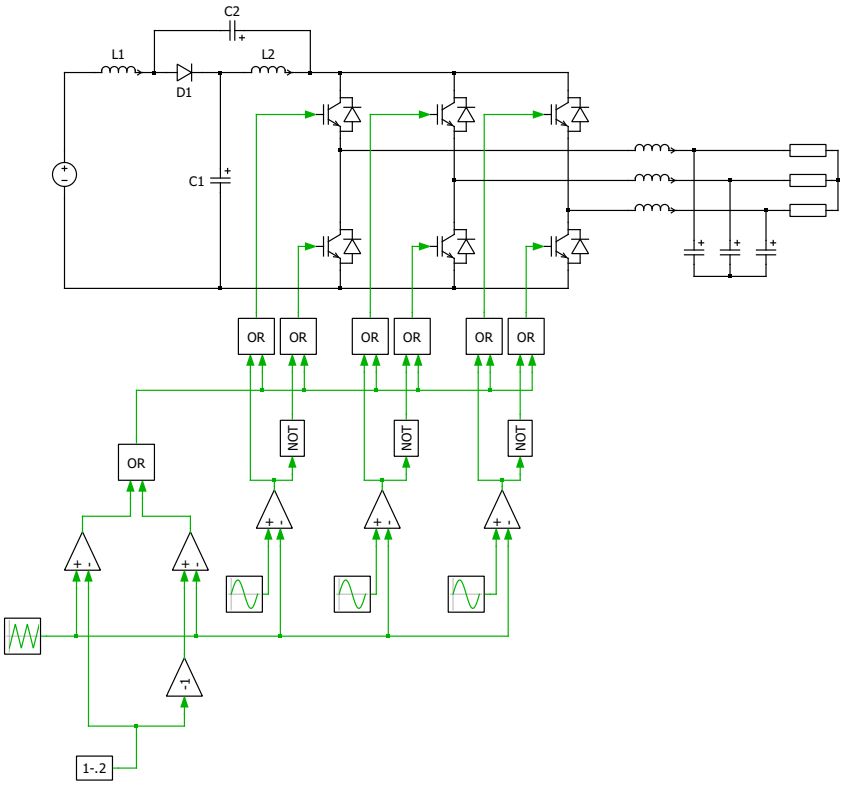


Figure 3.1: Simulation circuit of the simple boost control.

of the maximum boost control are shown in Figures 3.3 and 3.4, respectively.

In the maximum boost control, the shoot-through time per cycle is not constant, which means the boost factor is not constant. From Figure 3.4, we can see that the shoot-through duty ratio varies at six times of the output frequency, so there are low frequency ripples for inductor current and capacitor voltage, especially with a low output frequency [6]. Therefore, the requirement for passive components becomes high when the output frequency is low.

The maximum boost control scheme turns all traditional zero states into shoot-through states, inserting them when the triangular carrier wave is either greater than the maximum of all the sinusoidal references or smaller than the minimum of the references. Therefore, this method is able to obtain the maximum possible voltage boost for any given modulation index, so the maximum shoot-through duty ratio D_{max} can be deduced as $(1 - \frac{3\sqrt{3}M}{2\pi})$.

The scheme used in Figure 3.3 is based on this principle, finding the maximum and the minimum of the three reference sine waves and comparing these with the triangular carrier. With the simple boost control in Figure 3.1, the shoot-through

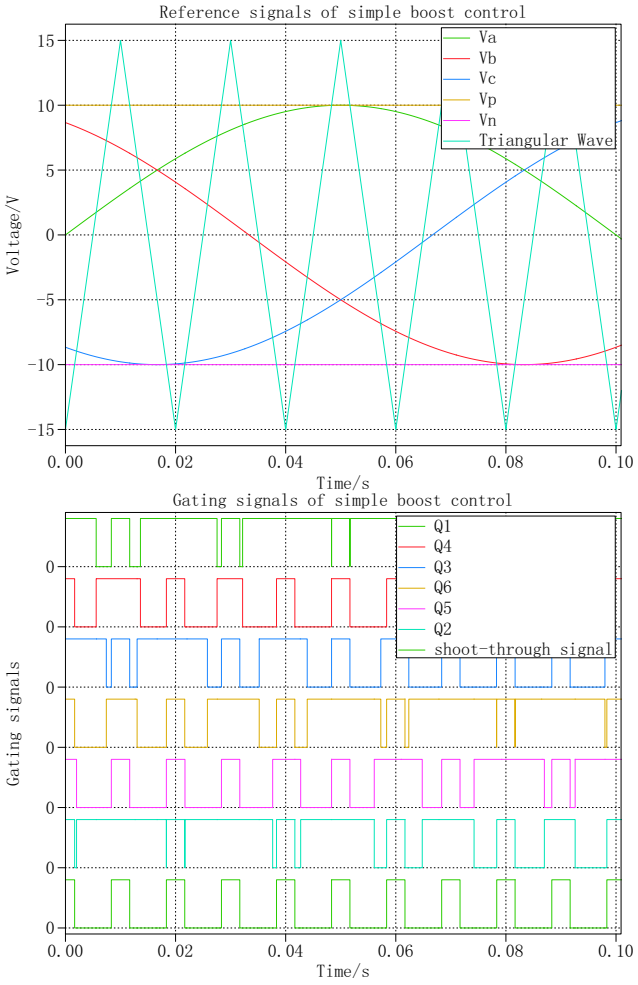


Figure 3.2: Control waveforms of the simple boost control.

signal is inserted in all 6 switching devices simultaneously, so that the three legs of the inverter are short-circuited at the same time.

3.2.3 Maximum Constant Boost Control

In order to minimize the cost and volume of the passive components, the low-frequency current ripple has to be eliminated. At the same time, it is often desirable to maximize the voltage boost for any given modulation index, in order to reduce the voltage stress across the switching devices. In the maximum boost control,

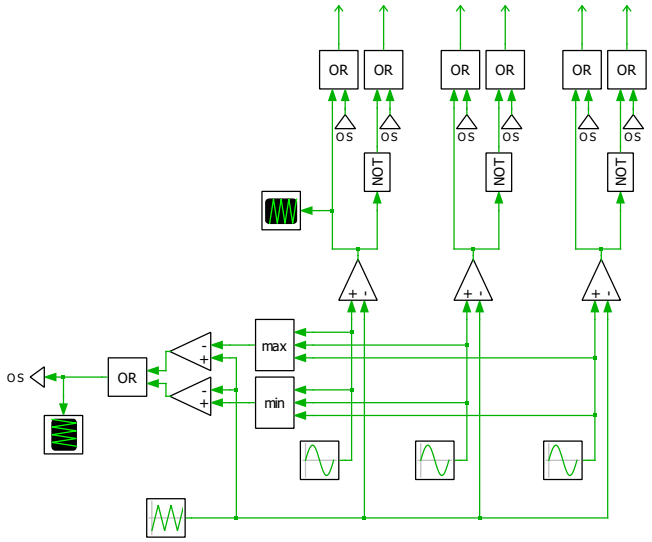


Figure 3.3: Simulation circuit of the maximum boost control.

the low-frequency current ripple is introduced because the shoot-through period is not kept constant. The maximum constant boost control method aims to achieve the maximum voltage gain while always maintaining the shoot-through duty ratio constant [10].

In the maximum constant boost control, the reference signals V_p and V_n are modified from the reference voltage of the MBC, in order to obtain a periodical shoot-through reference signal. These reference signals can be calculated according to the modulation index M and the amplitude of modulation waves [11]. The expressions used for these calculations are the following:

When $0 < \theta < \pi/3$:

$$V_{p1} = \sqrt{3}M + \sin(\theta - 2\pi/3)M \qquad V - n1 = \sin(\theta - 2\pi/3)M$$

When $\pi/3 < \theta < 2\pi/3$:

$$V_{p2} = \sin(\theta)M \qquad V_{n2} = \sin(\theta)M - \sqrt{3}M$$

The simulation circuit –only the PWM generator, the main circuit is the same as that shown in Figure 3.1– and the sketch map of maximum boost control are shown in Figures 3.5 and 3.6, respectively.

In the maximum constant boost control, the shoot-through time per switching cycle is constant. From Figure 3.6, we can see that the distance between the two shoot-through reference voltage curves is always the same as $\sqrt{3}M$, so the shoot-through duty ratio is $(2 - \sqrt{3}M)/2 = 1 - \sqrt{3}M/2$. The MCBC combines

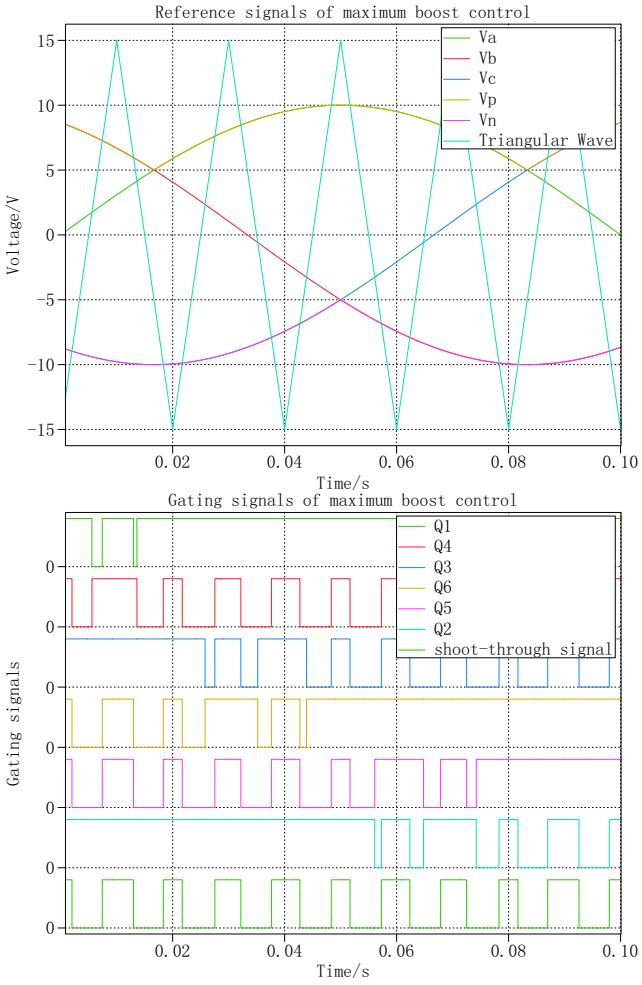


Figure 3.4: Control waveforms of the maximum boost control.

the advantages of the SBC and MBC, as it can achieve higher voltage gain of the qZSI than the simple boost control, and it has no low-frequency ripples on the voltage and current in the passive components, unlike the maximum boost control. Therefore, the requirement of passive components is reduced when compared to the MBC, and the switching devices are subjected to lower voltage stresses than those used in the SBC.

As seen in Figure 3.5, the procedure to implement the carrier-based maximum constant boost control is similar to the one used for the maximum boost control. However, instead of using the maximum and minimum of all three reference sine

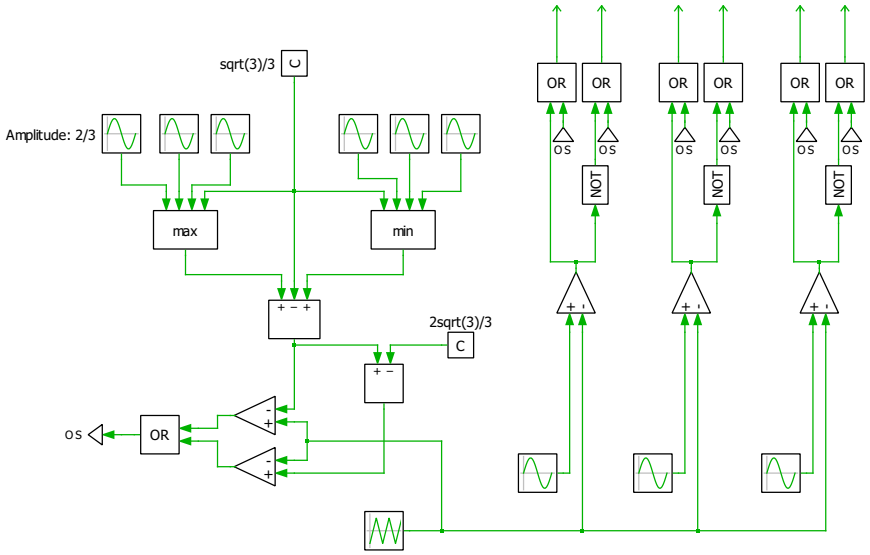


Figure 3.5: Simulation circuit of the maximum constant boost control.

waves as the shoot-through references directly, these are modified so as to maintain a constant distance between the shoot-through references.

To do so, three new reference sine waves are used, each with an amplitude of $2/3$ and centered at 0. A constant is used as a reference for the average value of the positive shoot-through reference. In the simulation used in Figure 3.5, this value is $\sqrt{3}/3$. After this, the maximum of the three reference waves and the constant is calculated. The same process is repeated to find the minimum of the constant and three reference waves with the same frequency and amplitude but biased to $2\sqrt{3}/3$. By adding these two signals together, a sine wave is obtained, with an average value of $2\sqrt{3}/3$. By subtracting $\sqrt{3}/3$ to it, its average value becomes $\sqrt{3}/3$. This signal is then used as the positive reference for the shoot-through calculation. It shares the same peaks as the positive reference used in the maximum boost control, but instead of dropping together with the maximum of the three reference sine waves, it is modified to be sinusoidal as well, as it can be seen by comparing V_p of Figure 3.6 and that of Figure 3.4. By shifting this shoot-through reference $-2\sqrt{3}/3$, the negative shoot-through reference V_n is obtained. By comparing these two references to the triangular carrier, the shoot-through signal is obtained. As with simple boost and maximum boost control, this signal is then inserted to the sinusoidal PWM signals driving the switching devices.

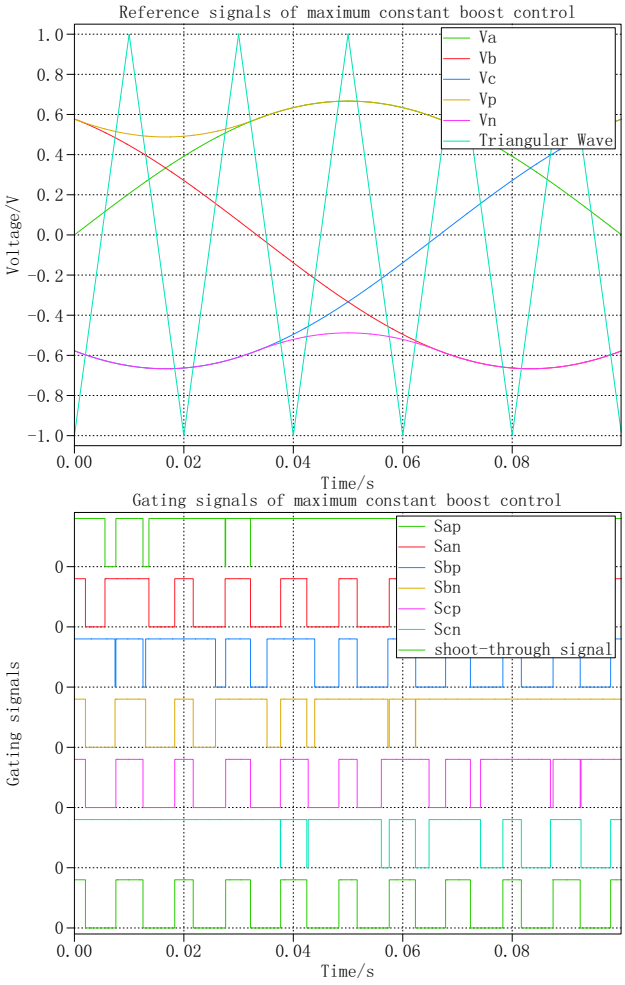


Figure 3.6: Control waveforms of the maximum constant boost control.

3.2.4 Comparison Between Carrier-based PWM Methods

The three analyzed carrier-based control methods for the qZSI all have their strengths and weaknesses:

- **Simple boost control** offers the lowest maximum shoot-through duty ratio and consequently voltage gain at any given modulation index, and also the highest switch voltage stress ratio. However, it is the simplest method to implement, as it requires the least modifications to the standard sinusoidal

PWM.

- **Maximum boost control** presents both the highest maximum voltage gain and the lowest switch voltage stress ratio. Thus, it would seem to be most efficient control method. However, as previously explained, a low output frequency causes unwanted low frequency current harmonics, and consequently, this control method increases the requirements for passive components. Therefore, it is often not suitable for applications that require a low or variable output frequency.
- **Maximum constant boost control** offers a compromise between the simple boost and maximum boost control schemes. It is able to achieve the maximum possible voltage gain while always maintaining a constant shoot-through duty ratio. As a result, it does not introduce undesirable harmonics. Therefore, the maximum constant boost control is often the most suitable for low or variable output frequency applications.

The comparison of the three modulation schemes can be found in Table 3.1 and Figures 3.7, 3.8, and 3.9, in terms of shoot-through duty ratio, voltage gain, and voltage stress.

Table 3.1: Maximum shoot-through duty ratio D_{max}, maximum voltage gain G_{max}, and maximum voltage stress V_s/V_{in} for the three analyzed carrier-based control methods for the qZSI [6].

	SBC	MBC	MCBC
$\mathbf{D_{max}}$	$1-M$	$1-\frac{3\sqrt{3}}{2\pi}M$	$1-\frac{\sqrt{3}}{2}M$
$\mathbf{G_{max}}$	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{M}{\sqrt{3}M-1}$
$\mathbf{V_s/V_{in}}$	$2G-1$	$\frac{3\sqrt{3}G}{\pi}-1$	$\sqrt{3}G-1$

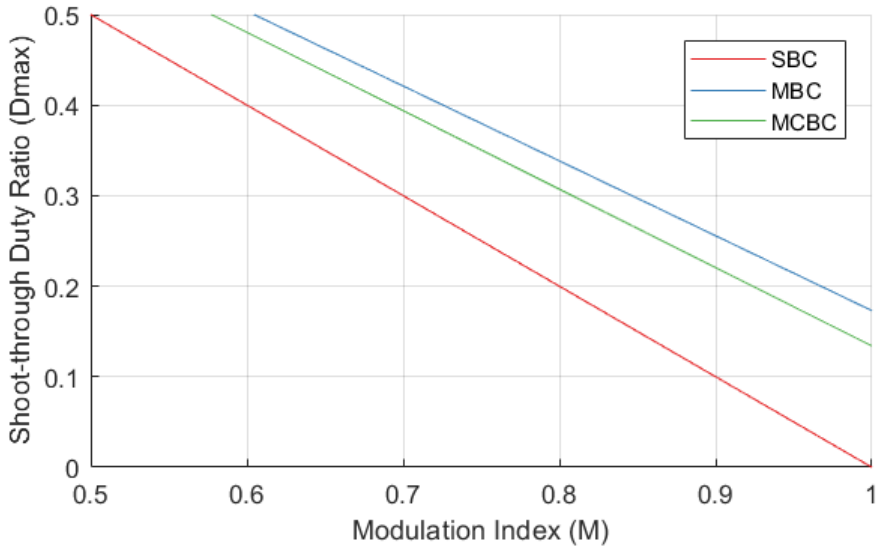


Figure 3.7: Maximum shoot-through ratio versus modulation index.

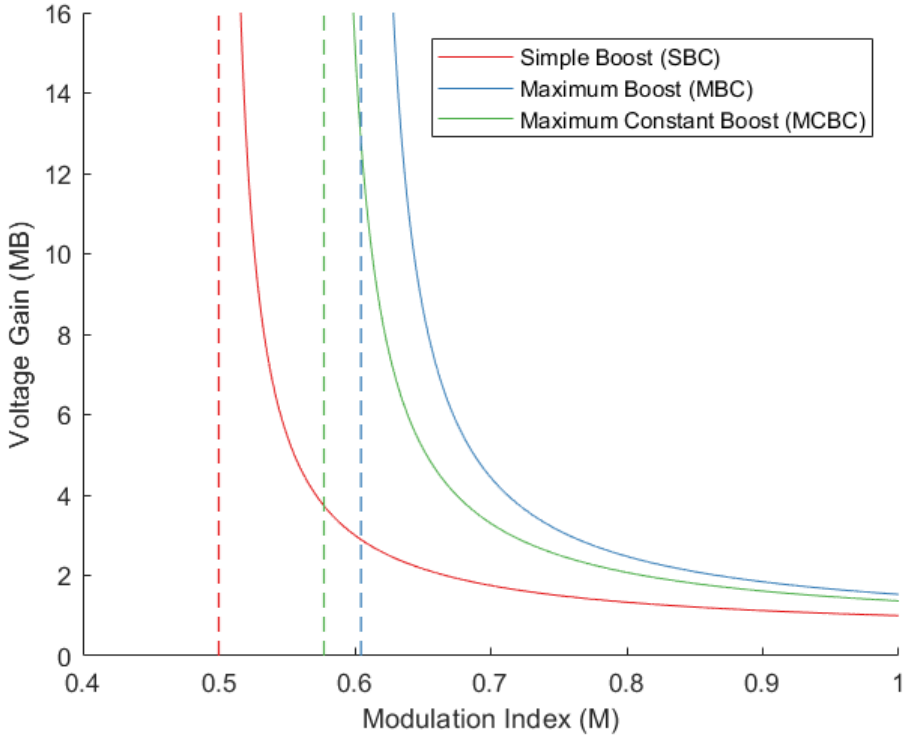


Figure 3.8: Maximum voltage gain versus modulation index.

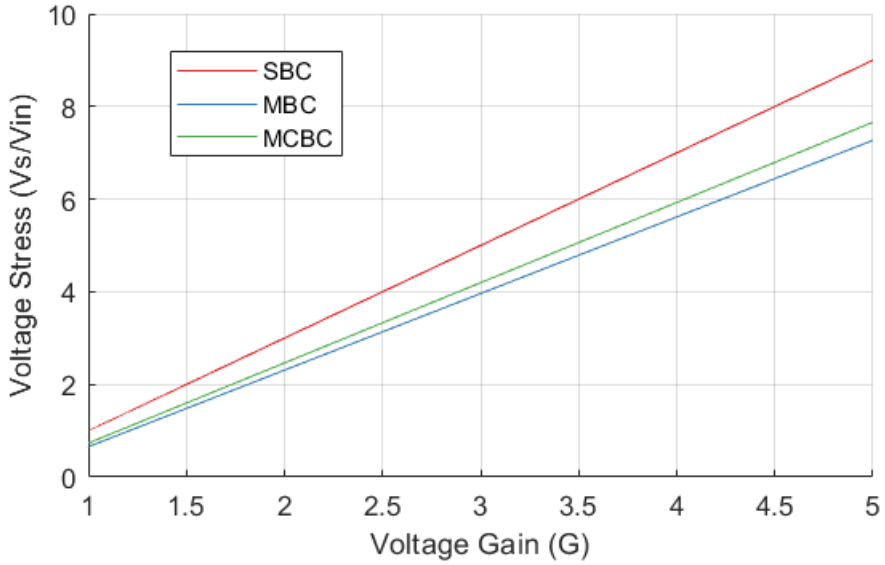


Figure 3.9: Voltage stress versus maximum voltage gain.

As shown in Figure 3.7, the simple boost control achieves the lowest maximum shoot-through duty ratio at any given modulation index when compared to the maximum boost control and maximum constant boost control. The highest maximum shoot-through duty ratio is achieved by maximum boost control.

When comparing the voltage gain, as shown in Figure 3.8, the maximum boost control method achieves the highest voltage gain at all modulation index than the other methods; whereas the simple boost control method requires a lower modulation index for the same maximum voltage gain. For all three methods, the voltage gain can theoretically increase to infinity at different values of M. For the simple boost control, this value is $\frac{1}{2}$, for the maximum boost control it is $\frac{\pi}{3\sqrt{3}}$, and for the maximum constant boost control, $\frac{1}{\sqrt{3}}$.

Regarding the voltage stress at the switching devices, as seen in Figure 3.9, at any given voltage gain, it is the highest for the simple boost control, and the lowest for maximum boost control. it can also be noted that for all three methods, voltage stress always increases linearly with the voltage gain.

3.3 Space Vector Pulse Width Modulation

The main purpose of the the classic inverter control is to make the output voltage of the inverter close to a sine wave with the desired characteristics. The space vector modulation is the name given to algorithms used for the digital implementation of the PWM control. The space vector modulation also differs from the carrier-based PWM in considering the inverter bridge as a single unit; whereas the carrier-based PWM can be considered as treating each leg of the bridge independently, each of them creating the waveform of every phase [9].

A traditional three-phase inverter, as shown in Figure 3.10, can be driven to eight unique states as shown in Table 3.2. It should be noted that the control of a standard voltage-source three-phase inverter always requires that the upper and lower switching devices of each leg should be in opposite states. Although having both devices of a leg gated off at the same time would not be particularly troublesome, gating them on simultaneously would lead to a short circuit and likely destroy the inverter.

Hence, there are $2^3 = 8$ possible states of the inverter, accounting for all possible combinations of switching states.

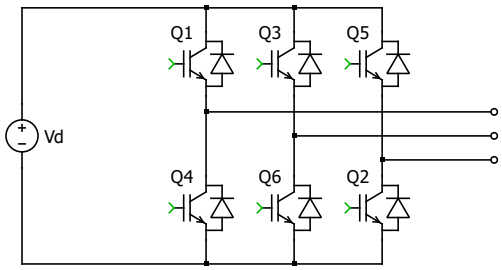


Figure 3.10: Standard voltage-fed three-phase inverter.

Table 3.2: Switching states of the standard three-phase voltage-source inverter.

State No.	Switch State	Q_1	Q_3	Q_5	Q_4	Q_6	Q_2	V_{ab}	V_{bc}	V_{ca}
1	100	ON	OFF	OFF	OFF	ON	ON	V_d	0	$-V_d$
2	110	ON	ON	OFF	OFF	OFF	ON	0	V_d	$-V_d$
3	010	OFF	ON	OFF	ON	OFF	ON	$-V_d$	V_d	0
4	011	OFF	ON	ON	ON	OFF	OFF	$-V_d$	0	V_d
5	001	OFF	OFF	ON	ON	ON	OFF	0	$-V_d$	V_d
6	101	ON	OFF	ON	OFF	ON	OFF	V_d	$-V_d$	0
7	111	ON	ON	ON	OFF	OFF	OFF	0	0	0
0	000	OFF	OFF	OFF	ON	ON	ON	0	0	0

In order to simplify the analysis of the system, a reference-frame transformation is used. This is based on the fact that any three-phase balanced voltages that satisfy:

$$v_a(t) + v_b(t) + v_c(t) = 0 \tag{3.5}$$

Can be expressed in a two-dimensional reference frame. This is due to the fact that any one of the three functions can be obtained by knowing the other two. In a balanced three-phase system, the voltage signals must satisfy equation 3.5. They can also be represented in a two-dimensional stationary space, for which the complex plane is normally used.

If the output voltages of each bridge leg of the three-phase voltage-source inverter are V_a, V_b and V_c, the composite voltage vector generated by the inverter is [4]:

$$\vec{V} = \frac{2}{3}(V_a + e^{j2\pi/3}V_b + e^{j4\pi/3}V_c) \tag{3.6}$$

where $\vec{V}$ is a rotating space vector in a complex notation. $\vec{V}$ can be expressed in real and imaginary components as:

$$\vec{V} = v_x + jv_y \tag{3.7}$$

Using equations 3.6 and 3.7, the reference transformation can be obtained as:

$$\begin{bmatrix} v_x \\ v_y \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.8}$$

Which can be used for balanced systems that satisfy equation 3.5.

Space vector. The three-phase VSI can generate 8 voltage vectors, which can be defined as such:

$$\vec{V} = 2V_{PN}e^{j(k-1)\pi/3}/3 \qquad k = 1,2,3,4,5,6 \tag{3.9}$$

$$\vec{V} = 0 \qquad k = 0,7 \tag{3.10}$$

The following rules are obeyed [13]:

$$\begin{aligned} \vec{V}_1 &= -\vec{V}_4 \\ \vec{V}_2 &= -\vec{V}_5 \\ \vec{V}_3 &= -\vec{V}_6 \\ \vec{V}_0 &= \vec{V}_7 = \vec{0} \\ \vec{V}_1 + \vec{V}_3 + \vec{V}_5 &= \vec{0} \end{aligned} \tag{3.11}$$

We use 000, 100, 110, 010, 011, 001, 101, 111 to represent every voltage vector, where 1 and 0 means that the upper switching device of each bridge leg turns on and off, respectively.

The vector space is divided into 6 sectors, as shown in Figure 3.11, where: V_{PN} is the DC-link voltage, V^* is the reference vector $\vec{V}$, T_s is the switching cycle, T_1 is the working time of V_1, T_2 is the working time of V_2, T_0 is the working time of the zero vector, and θ is the angle between V^* and V_1.

The output voltage vector $\vec{V}^*$ in one sampling interval can be expressed as:

$$\vec{V}(t) = \frac{T_0}{T_s}\vec{V}_0 + \frac{T_1}{T_s}\vec{V}_1 + \ldots + \frac{T_7}{T_s}\vec{V}_7 \tag{3.12}$$

where $T_0, T_1, \ldots, T_7 \geq 0$ are the turn-on time of vectors $\vec{V}_0, \vec{V}_1, \ldots, \vec{V}_7$; $T_0 + T_1 + \ldots + T_7 = T_s$, and T_s is the sampling time.

The reference vector $\vec{V}$ is commonly split into the two nearest voltage vectors and the two zero vectors in an arbitrary sector. For instance, in sector I, this decomposition leads to the expression:

$$\vec{V} = \frac{T_1}{T_s}\vec{V}_1 + \frac{T_2}{T_s}\vec{V}_2 + \frac{T_7}{T_s}\vec{V}_7 + \frac{T_0}{T_s}\vec{V}_0 \tag{3.13}$$

Assuming $\vec{V}$ to be at sector I, the reference voltage vectors can be defined as such:

$$\vec{V}_1 = \frac{2}{3}V_{PN}; \quad \vec{V}_2 = \frac{2}{3}V_{PN}e^{j\pi/3}; \quad \vec{V}_z = 0; \quad \vec{V} = Ve^{j\theta} \tag{3.14}$$

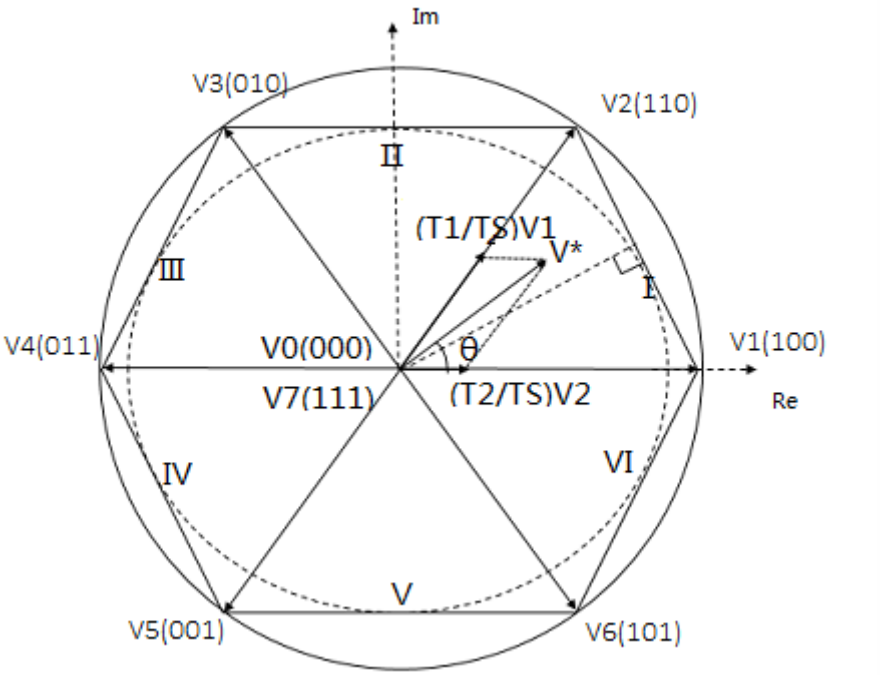


Figure 3.11: Voltage space vector diagram.

where $\vec{V}_z$ and subsequently T_z are considered to be the combination of both zero states $\vec{V}_0$ and $\vec{V}_7$. Thus, from equation 3.13:

$$T_s V e^{j\theta} = T_1 \frac{2}{3} V_{PN} + T_2 \frac{2}{3} V_{PN} e^{j\pi/3} + T_z \times 0 \tag{3.15}$$

Converting into rectangular coordinates and equating the real and imaginary parts on both sides:

$$T_s V(\cos\theta + j\sin\theta) = T_1 \frac{2}{3} V_{PN} + T_2 \frac{2}{3} V_{PN}(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}) + T_z \times 0 \tag{3.16a}$$

$$T_s V\cos\theta = T_1 \frac{2}{3} + T_2 \frac{2}{3}\cos\frac{\pi}{3} + Tz \times 0 \tag{3.16b}$$

$$jT_s V\sin\theta = jT_2 \frac{2}{3} V_{PN}\sin\frac{\pi}{3} \tag{3.16c}$$

Solving for T_1, T_2, and T_z for the first sector ($0 \leq \theta \leq \pi/3$), the expressions for

these parameters can be derived as [9]:

$$T_1 = \frac{\sqrt{3}T_s V}{V_{PN}} \sin\left(\frac{\pi}{3} - \theta\right) = T_s M \sin\left(\frac{\pi}{3} - \theta\right) \tag{3.17a}$$

$$T_2 = \frac{\sqrt{3}T_s V}{V_{PN}} \sin\theta = T_s M \sin\theta \tag{3.17b}$$

$$T_z = T_s - T_1 - T_2 \tag{3.17c}$$

where M is the modulation index for the SVPWM, which is equal to $\sqrt{3}V^*/V_{PN}$, with V being the peak reference value, related to its rms value by $\sqrt{2}$.

As can be deduced from equations 3.17a and 3.17b, in sector I, the dwell times T_1 and T_2 will be equal if the reference voltage vector $\vec{V}$ lies exactly in the middle of $\vec{V_1}$ and $\vec{V_2}$ ($\theta = \pi/6$). If $\vec{V}$ lies completely on $\vec{V_1}$ ($\theta = 0$), the dwell time T_2 will be zero; and if $\vec{V}$ lies completely on $\vec{V_2}$ ($\theta = \pi/3$), the dwell time T_1 will be zero.

Assuming the output frequency to be constant, equations 3.17a, 3.17b, and 3.17c are still applicable for the calculations of dwell times in the other 5 sectors, as long as a modified angle θ_k for the kth sector is used instead of θ as:

$$\theta_k = \theta - (k-1)\frac{\pi}{3} \quad \text{for } 0 \leq \theta_k \leq \frac{\pi}{3} \tag{3.18}$$

As the hexagon formed by the 6 sectors of the SVM scheme is formed by six stationary vectors with a length of $2V_{PN}/3$, the maximum value of the reference vector $\vec{V}$ is given by:

$$V_{r,max} = \frac{2}{3}V^* \frac{\sqrt{3}}{2} = \frac{V^*}{\sqrt{3}} \tag{3.19}$$

Therefore, the maximum modulation index for SVM is:

$$M_{max} = \frac{\sqrt{3}}{V} \frac{V}{\sqrt{3}} = 1 \tag{3.20}$$

Thus, the modulation index for the SVM can range from 0 to 1 in normal operation mode. Further increasing M leads to overmodulation, which as shown for the carrier-based PWM allows for more utilization of the DC input voltage. However, overmodulation also causes a high degree of distortion in output voltages, resulting in non-sinusoidal signals. This is especially true for low output frequencies. The distortion introduced by overmodulation is due to the fact that $\vec{V}$ exceeds the size of the hexagon, and as such $T_1 + T_2$ becomes greater than T_s, rendering the inverter unreliable [13].

As previously mentioned, the dwell time T_z is equal to the sum of the dwell times of both zero states, T_0 and T_7. As such, there is a degree of freedom in the distribution of the dwell times of both states. Assuming linear modulation range ($0 \leq M \leq 1$), $T_z \geq 0$. For continuous space-vector schemes, both zero states

are used, resulting in positive dwell times T_0 and T_7. For discontinuous space-vector schemes, only one of the two zero states is used, resulting in the dwell time corresponding to the other zero state being equal to 0.

In general, the time interval corresponding to the zero states (T_z) is evenly distributed between the two zero states. Therefore:

$$T_0 = \frac{T_z}{2}, \quad T_7 = \frac{T_z}{2} \tag{3.21}$$

The space vector sequence can then be generated as shown in Figure 3.12, using the first sector as an example. The switching sequences for all six sectors are shown in Table 3.3.

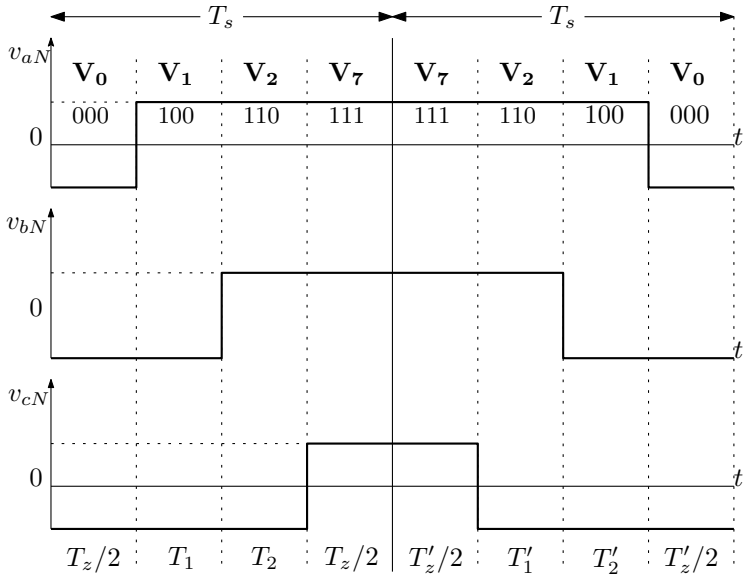


Figure 3.12: Pattern of the space vector modulation sequence [9].

For the digital implementation of the SVM, the following algorithm can be used [9]:

1. Use the a-b-c to α-β transformation to obtain the two components of the reference voltage $\vec{V}$.
2. Calculate the magnitude V and the angle θ of the reference voltage $\vec{V}$.
3. Find the sector angle θ_k using equation 3.18.
4. Calculate the modulation index M.
5. Determine the dwell times T_1, T_2, and T_z from equations 3.17a, 3.17b, and 3.17c.
6. Find the gating sequence using Table 3.3.

Table 3.3: Switching sequences for all SVM sectors [9].

	Switching Segment						
Sector	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1	V_0	V_1	V_2	V_7	V_2	V_1	V_0
	000	100	110	111	110	100	000
2	V_0	V_3	V_2	V_7	V_2	V_3	V_0
	000	010	110	111	110	010	000
3	V_0	V_3	V_4	V_7	V_4	V_3	V_0
	000	010	011	111	011	010	000
4	V_0	V_5	V_4	V_7	V_4	V_5	V_0
	000	001	011	111	011	001	000
5	V_0	V_5	V_6	V_7	V_6	V_5	V_0
	000	001	101	111	101	001	000
6	V_0	V_1	V_6	V_7	V_6	V_1	V_0
	000	100	101	111	101	100	000

3.3.1 Standard SVM Implementation

An example of the implementation in *PLECS* of the standard SVM method used is shown in Figures 3.13 to 3.18. As seen in Figure 3.13, the inverter circuit requires no modifications with respect to the one used in the carrier-based PWM.

The *SVPWM Generator* block, shown in Figure 3.14 is tasked with obtaining the six switching signals corresponding to each of the switching devices, by following the algorithm previously stated. Therefore, the block requires three output voltage reference signals and the period of the switching devices.

The first step is then to obtain the reference output voltage vector $\vec{V}$ and calculate its magnitude V_r and angle θ. All the angles used in this simulation are expressed in degrees. To find θ a ramp is used with a slope of $360^\circ \times f$. The block representation of this scheme is shown in Figure 3.15.

The next step is to find the sector number k and the sector angle θ_k. This is done by comparing the angle θ to the angles of the reference voltages $V_1, V_2, V_3, V_4, V_5, V_6$, as shown in Figure 3.11. Once the sector number has been found, the modified angle θ_k can be calculated using equation 3.18.

Afterwards, the value of the modulation index M must be found, by dividing

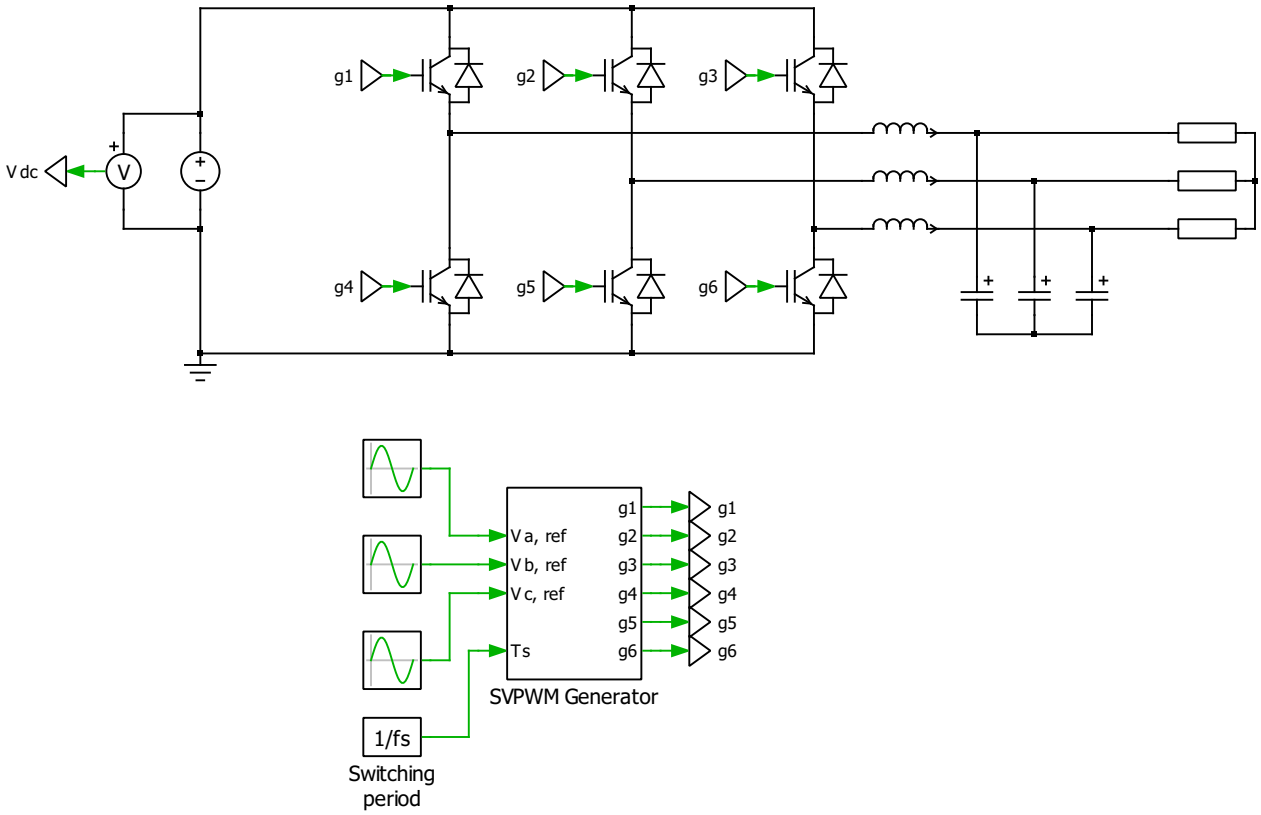


Figure 3.13: Voltage-source three-phase inverter and control block.

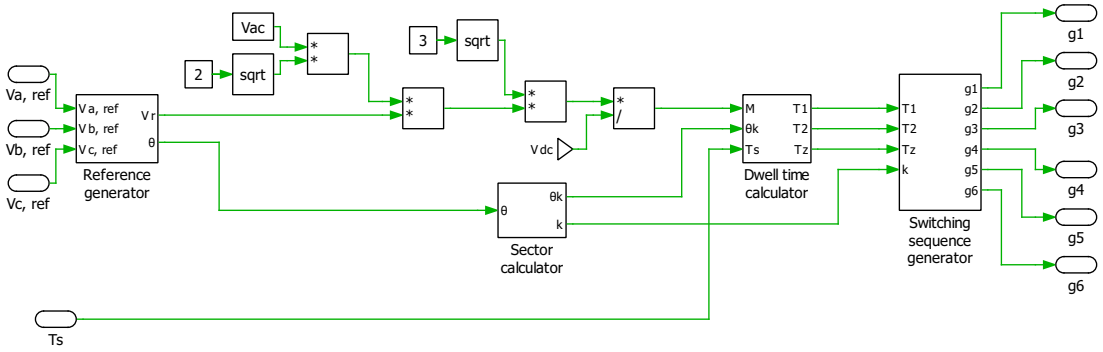


Figure 3.14: Control block for the space vector modulation.

the peak value of the desired output voltage V_{ac} over the input voltage V_{PN}.

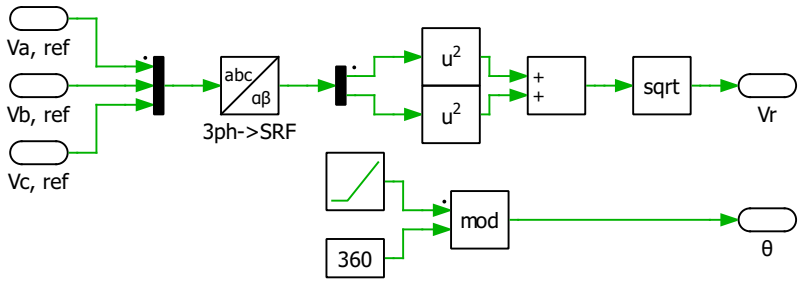


Figure 3.15: Reference generator.

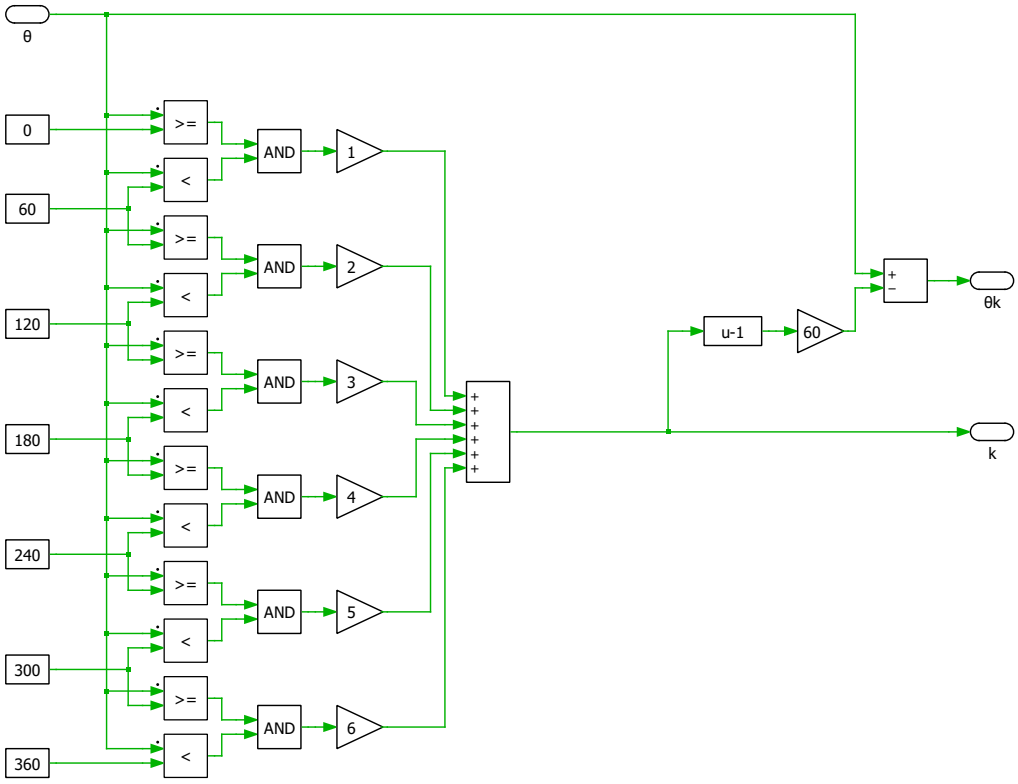


Figure 3.16: Sector calculator.

The dwell time calculator block, shown in Figure 3.17, can then find the values of the dwell times T_1, T_2, and T_z by using the previously calculated modulation index M, sector angle θ_k and the given switching period T_s. To do so, the block diagram is based on equations 3.17a, 3.17b, and 3.17c.

Finally, the six gating signals can be obtained from the three dwell times and sector angle k, as shown in Figure 3.18. For that purpose, the calculations are based on Table 3.3. In this case, the total zero state dwell time T_z is assumed to be evenly

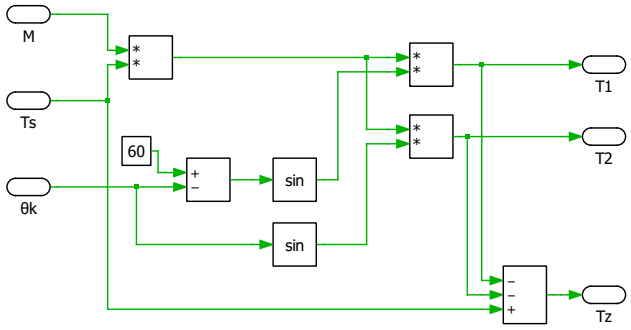


Figure 3.17: Dwell time calculator.

split between the two zero states, as shown in equation 3.21.

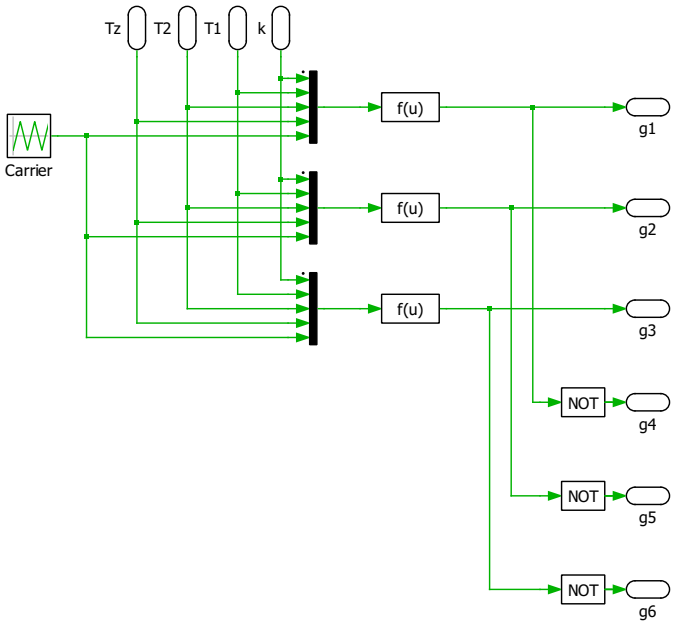


Figure 3.18: Switching sequence generator.

3.3.2 SVM for qZSI

Space vector modulation can also be applied to Z-source/quasi-Z-source inverters, utilizing its benefits of high DC-link voltage utilization and low output harmonics, as well as efficiency for digital implementation. The qZSI adds another voltage vector to the six active vectors and two zero vectors of the traditional voltage-source inverter, corresponding to the shoot-through zero vector. As a result, the SVM scheme used for traditional voltage-source inverters must be modified accordingly

in order to make use of the voltage boosting capabilities of the qZSI. Most of the control scheme remains the same, essentially modifying only the switching sequence to include the shoot-through state.

By inserting the shoot-through zero vector, the reference voltage vector $\vec{V}^*$ becomes [5]:

$$\vec{V} = \frac{T_1 V_1}{T_s} + \frac{T_2 V_2}{T_s} + \frac{T_0 V_0}{T_s} + \frac{T_{sh} V_{sh}}{T_s} \tag{3.22}$$

where V_{sh} is the shoot-through voltage vector, while V_{sh} and V_0 will not affect $\vec{V}$. Since $T_1 + T_2 \leq T_s$, $\vec{V} \leq \sqrt{3}V_1/2$ and $D = T_{sh}/T_s \leq 1 - 2\vec{V}/\sqrt{3}$.

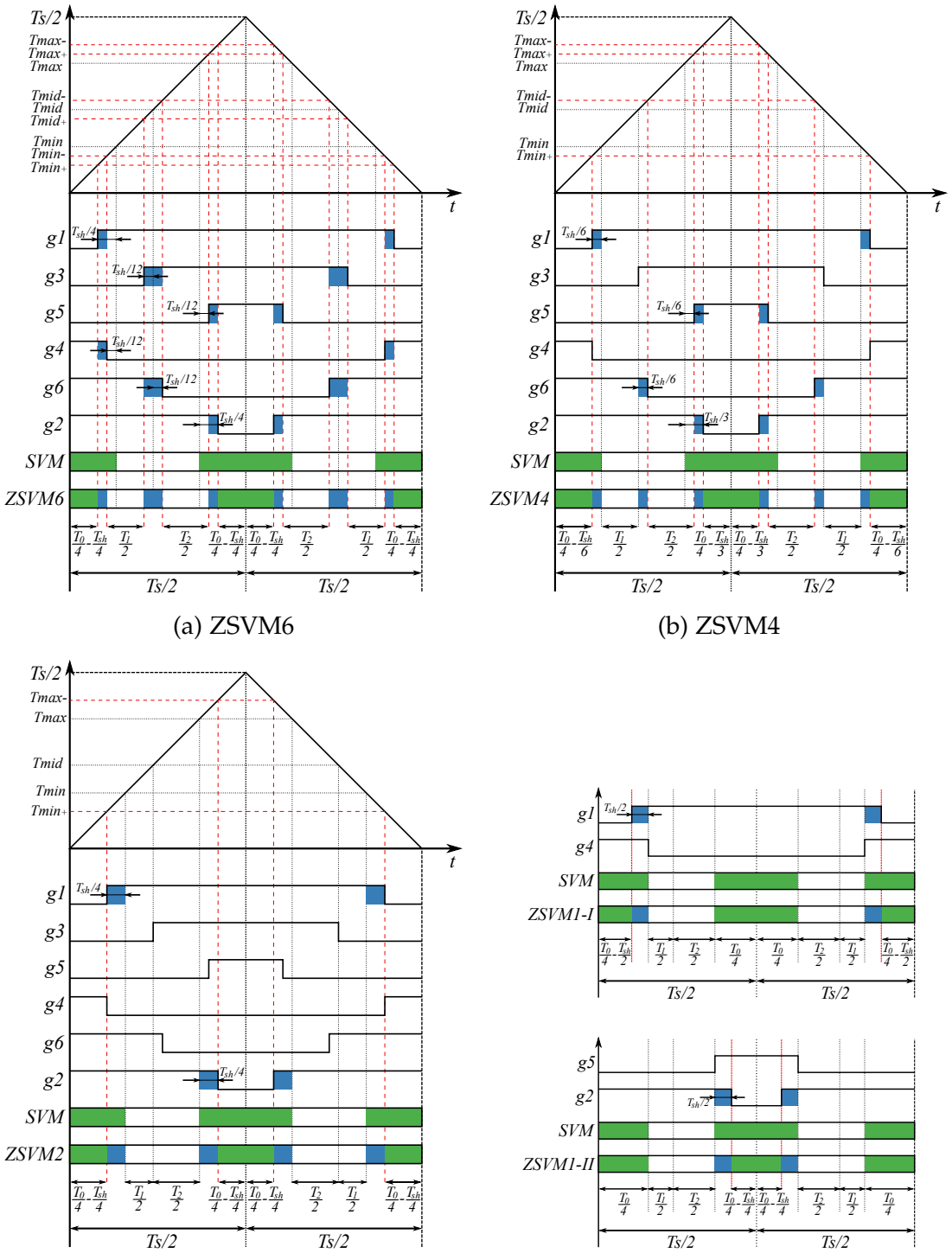
In traditional SVM, using T_{min}, T_{mid} and T_{max} to represent the the switching time for three legs, then $T_{min} = T_0/4$, $T_{mid} = T_0/4 + T_1/2$ and $T_{max} = T_S/2 - T_0/4$. To make the reference output voltage $\vec{V}$ remain constant, T_{sh} must only occupy time from T_0, so that T_1 and T_2 always maintain the same values as in the traditional SVM. To minimize losses, all the switching devices should only be turned on and off once per switching period. This will be a defining characteristic of the modified SVM methods, as carrier-based PWM methods modified with shoot-through signals could introduce more switching states.

Depending on how the shoot-through time is distributed in the switching states, there are several types of SVMs for qZSI, as shown in Figure 3.19 [5]. These modulation methods are commonly referred to as $ZSVMx$, where x refers to the number of modified switching signals in each switching semi-period.

- **ZSVM6**. The shoot-through period T_{sh} is inserted into all 6 switching states. Every shoot-through period lasts for $T_{sh}/6$. It can also be deduced that there is a relationship between T_{sh} and T_0: $T_0/4 - T_{sh}/4 \geq 0$, which means that $T_{sh} \leq T_0$, as shown in Figure 3.19(a). This means that the entire traditional zero state can be substituted by the shoot-through state.

- **ZSVM4**. The shoot-through period is inserted into four of the six switching states, with each shoot-through lasting for $T_{sh}/6$. Although the resulting signals from ZSVM4 look quite similar to those from ZSVM6, ZSVM4 still uses the traditional T_{min} and T_{mid} references, whereas ZSVM6 only uses the modified ones for all switching times. In this case, as shown in Figure 3.19(b), $T_0/4 - T_{sh}/3 \geq 0$, and therefore $T_0 \geq 3T_0/4$.

- **ZSVM2**. In this case, the shoot-through period is inserted in two of the traditional states, each with a value of $T_{sh}/4$. As a consequence, the reference time T_{mid} is not modified, so that one of the inverter legs operates without shoot-through in each sector. As with ZSVM6, $T_0/4 - T_{sh}/4 \geq 0$, so the entire traditional zero state can become a shoot-through state ($T_{sh} \leq T_0$), as observed in Figure 3.19(c).



(a) ZSVM6

(b) ZSVM4

(c) ZSVM2

(d) ZSVM1-I & ZSVM1-II

Figure 3.19: Space vector modulation methods for the qZSI.

- **ZSVM1**. In this modulation scheme, the shoot-through state is only inserted in one of the zero states. As such, there are two variants of the ZSVM1:
  - **ZSVM1-I**, where the shoot-through state is completely inserted in the 000 (T_0) zero state.
  - **ZSVM1-II**, where the shoot-through state is completely inserted in the 111 (T_7) zero state.

  The two variants of the ZSVM1 share most of their characteristics, with the shoot-through period lasting for $T_0/2$. As seen in Figure 3.19(d), $T_0/4 - T_{sh}/2 \geq 0$, and therefore $T_{sh} \leq T_0/2$.

Using the SVM for the qZSI generally shows a better performance than the one obtained from the modified carrier-based modulation methods. The SVM is also easier to manipulate, as it is intended for use as a digital PWM method.

3.4 Summary

Major parameters to be considered when designing the control scheme for a qZSI are shown in Table 3.4. It should be noted that the carrier-based maximum boost control and the SVM methods ZSVM6 and ZSVM2 all share many of their parameters, despite their different implementations.

The maximum shoot-through duty ratio D_{max} can be calculated by analyzing the procedure used in the implementation of each modulation method. The maximum voltage gain G_{max} can be found by multiplying the modulation index M with the maximum boost factor B_{max}, where B_{max} is defined as:

$$B_{max} = \frac{1}{1 - 2D_{max}} \tag{3.23}$$

Voltage stress at the inverter legs can be calculated using the qZSI circuit analysis together with the voltage gain.

The expressions shown in Table 3.4 can then be graphed to ease their comparison, resulting in Figures 3.20, 3.21, and 3.22.

In all of the analyzed modulation techniques for the ZSI/qZSI, there is inverse proportionality between the maximum allowable shoot-through duty ratio D_{max} and the used modulation index M.

When considering the studied ZSVM techniques, Figure 3.20 shows that both the ZSVM1 and ZSVM4 allow for lower shoot-through duty ratios than the ZSVM6 and ZSVM2. At low modulation index, both the ZSVM1 and ZSVM4 only allow

Table 3.4: Maximum shoot-through duty ratio D_{max}, maximum voltage gain G_{max}, and voltage stress V_s/V_{in} associated with the different modulation methods that have been studied [5].

	SBC	MCBC	MBC/ZSVM6/ZSVM2	ZSVM4	ZSVM1
D_{max}	$1-M$	$1-\frac{\sqrt{3}}{2}M$	$1-\frac{3\sqrt{3}}{2\pi}M$	$\frac{3}{4}(1-\frac{3\sqrt{3}}{2\pi}M)$	$\frac{1}{2}(1-\frac{3\sqrt{3}}{2\pi}M)$
G_{max}	$\frac{M}{2M-1}$	$\frac{M}{\sqrt{3}M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{4\pi M}{9\sqrt{3}M-2\pi}$	$\frac{2\pi}{3\sqrt{3}}$
V_s/V_{in}	$2G-1$	$\sqrt{3}G-1$	$\frac{3\sqrt{3}G}{\pi}-1$	$\frac{9\sqrt{3}G}{2\pi}-2$	$\frac{2\pi}{3\sqrt{3}M}$

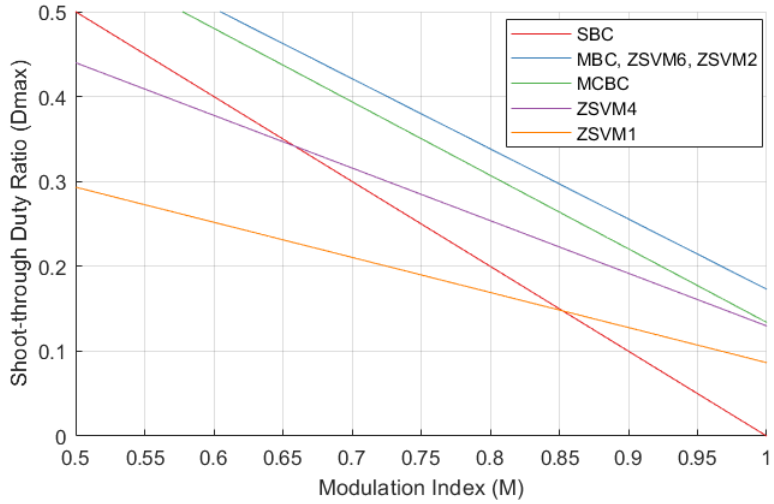


Figure 3.20: Maximum shoot-through duty ratio versus modulation index for all considered modulation methods.

for lower shoot-through duty ratios than the simple boost carrier-based PWM. The ZSVM1 presents the lowest D_{max} values out of all the ZSVM methods.

It should be noted that while the carrier-based PWM methods can operate in the over-modulation region by increasing M to be values higher than 1, the equations used to calculate the maximum shoot-through duty ratio and maximum voltage gain do not hold, and therefore, are not plotted in Figure 3.20. For SVM methods, their ability to operate in the overmodulated region ($1 < M < 2/\sqrt{3}$) is more limited, as it depends on whether the implementation of the SVM algorithm considers the possibility of overmodulation, which modifies the calculation of dwell times in order to prevent them from taking negative values.

The maximum voltage gain, as shown in Figure 3.21 is only dependent on the

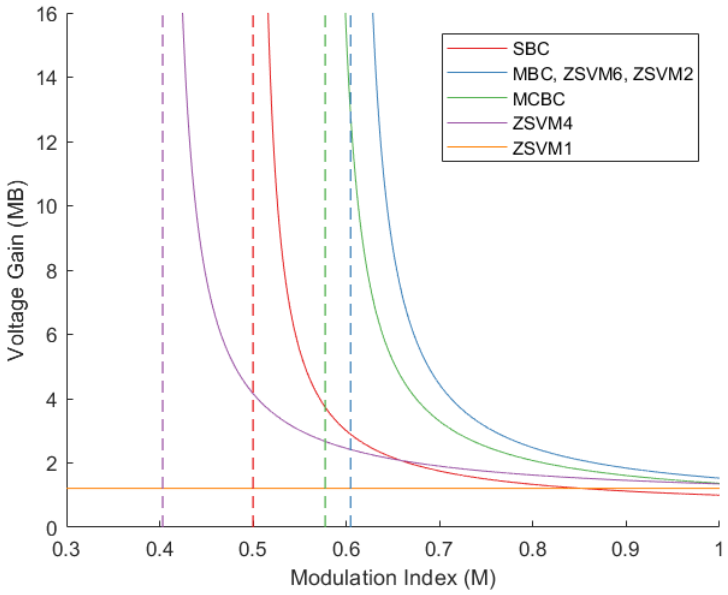


Figure 3.21: Maximum voltage gain versus modulation index for all considered modulation methods.

modulation index M. The curve for the ZSVM4 has a hyperbolic shape similar to that of the carrier-based modulation methods, while the ZSVM6 and ZSVM2 present a maximum voltage gain identical to that of the maximum boost control. The ZSVM4, however, offers the lowest maximum voltage gain at a lower modulation index apart from the ZSVM1. The ZSVM4 reaches theoretically an infinite maximum voltage gain at a modulation index of $M = \frac{2\pi}{9\sqrt{3}} \approx 0.403$.

Unlike all the other considered modulation methods, the ZSVM1 presents a constant maximum voltage gain for all values of M, its value being $B_{max} = \frac{2\pi}{3\sqrt{3}} \approx 1.21$. Therefore, the maximum voltage stress associated with the ZSVM1 as shown in Table 3.4 does not depend on the maximum voltage gain, and is instead only inversely proportional to the modulation index M. Hence, its plot is not shown in Figure 3.22. From its mathematical expression, however, it can be deduced that the maximum voltage stress of the ZSVM1 has a hyperbolic shape, with theoretically infinite stresses at $M = 0$ and zero stresses at $M \to \infty$.

The correlation between the maximum voltage stress and maximum voltage gain implies that the lower the voltage gain at a given modulation index is, the higher the voltage stress will be. As shown in Figure 3.22, the ZSVM4 offers the lowest voltage stress at low voltage gains. However, as the gain is increased, it is quickly overtaken by the other methods. As a result, at higher voltage gains, the ZSVM6, ZSVM2 and MBC offer the lowest maximum voltage stress, closely

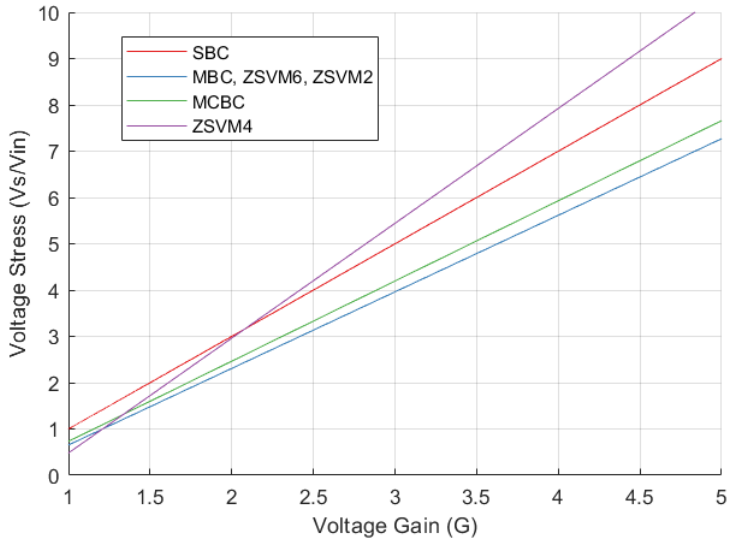


Figure 3.22: Voltage stress versus voltage gain for all considered modulation methods.

followed by the MCBC.

Although the carrier-based maximum boost control shares many of its parameters with the ZSVM6 and ZSVM2, the SVM methods are able to maintain the shoot-through time constant in every switching cycle, thus avoiding the high distortion introduced by the maximum boost control. The main difference between the ZSVM2 and ZSVM6 is that the shoot-through period in the ZSVM2 is only inserted in the zero-states, while ZSVM6 also introduces shoot-through in the middle switching moment.

Chapter 4

Experimental Tests

This chapter shows the equipment setup, procedures, and results of the experiments regarding the operation and voltage boost capabilities of the quasi-Z-source inverter.

4.1 Experimental Setup

Figure 4.1 shows the main hardware used for the experimental tests, consisting of the inverter bridge, impedance source network, load, and signal processing devices; both for inverter control inputs and for output measurements.

Each of the main components used in the experiments, as shown in figure 4.1 can be listed as such:

- **DSP**: A DSP (digital signal processor) is a unique microprocessor that uses digital signals to process large amounts of information. Its working principle is to receive analog signals and convert them to binary digital signals. Then the digital signal is modified, deleted, enhanced, and the digital data is interpreted back to the analog data or the actual environment format in other system chips. Not only is it programmable, but its real-time operating speed can reach tens of millions of complex instruction programs per second. In this experiment, the DSP model that we use is the Texas Instruments F28335 Delfino Microcontroller.
- **FPGA**: An FPGA (Field-Programmable Gate Array) is a microprocessor based on PAL, GAL, CPLD and other programmable devices. It emerged as a type of semi-custom circuit in the application-specific integrated circuit (ASIC) field. It allows the user to configure logic gates in any desired way. In the

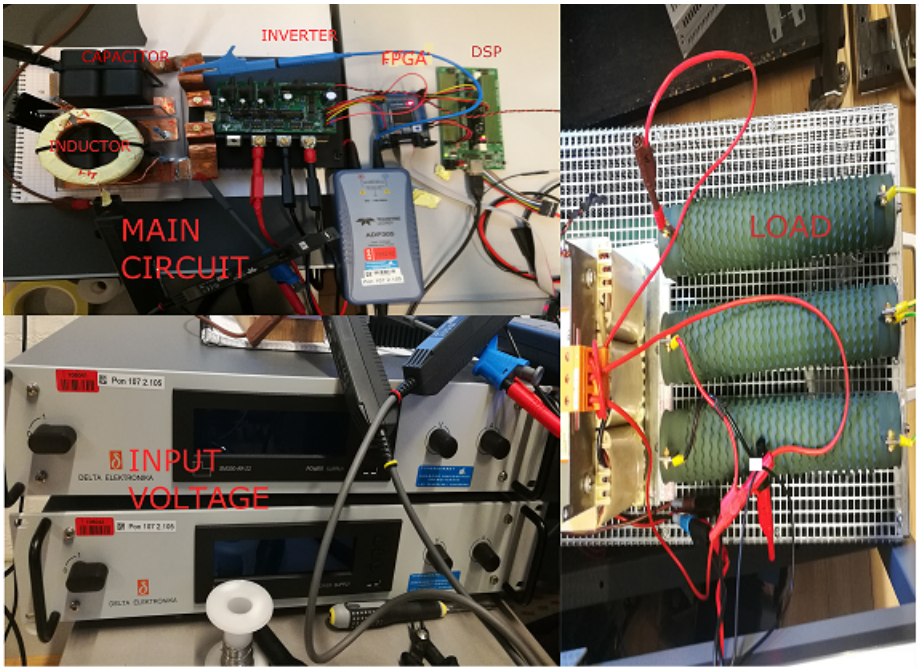


Figure 4.1: The hardware used in the performed experiments.

performed experiments, the FPGA is used to introduce the shoot-through states to the simple boost control scheme, as the DSP is not able to perform logic gate calculations. For the SVM, however, no FPGA will be required, as the output signals from the DSP already include the shoot-through states. The FPGA model used is an Altera Cyclone IV, and its implemented program for the simple boost control is shown in Figure 4.2.

- **Inverter**: We use a Mitsubishi Electric PM75RL1A120 IGBT-based unlocked inverter package which consists of the inverter bridge, braking circuit and drivers, and protection IC. It uses an IGBT-based inverter bridge and it is rated at 1200 V and 75 A, far above the values used in the performed experiments. It is connected to the impedance network and receives its gating signals from the DSP/FPGA. The inverter package requires an input signal of 24 V DC in order to drive the IGBTs, as the gating signals coming from the DSP/FPGA outputs are limited at 3.3 V, which is an insufficient voltage to drive them on its own.
- **Inductor**: Each one of the two inductors constituting the quasi-Z-source network has an inductance rating of 300 μH.
- **Capacitor**: Each one of the two capacitors has a capacitance rating of 100 μF.
- **Diode**: A power diode is also used in the series connection of the two inductors, as shown in the qZSI diagrams.

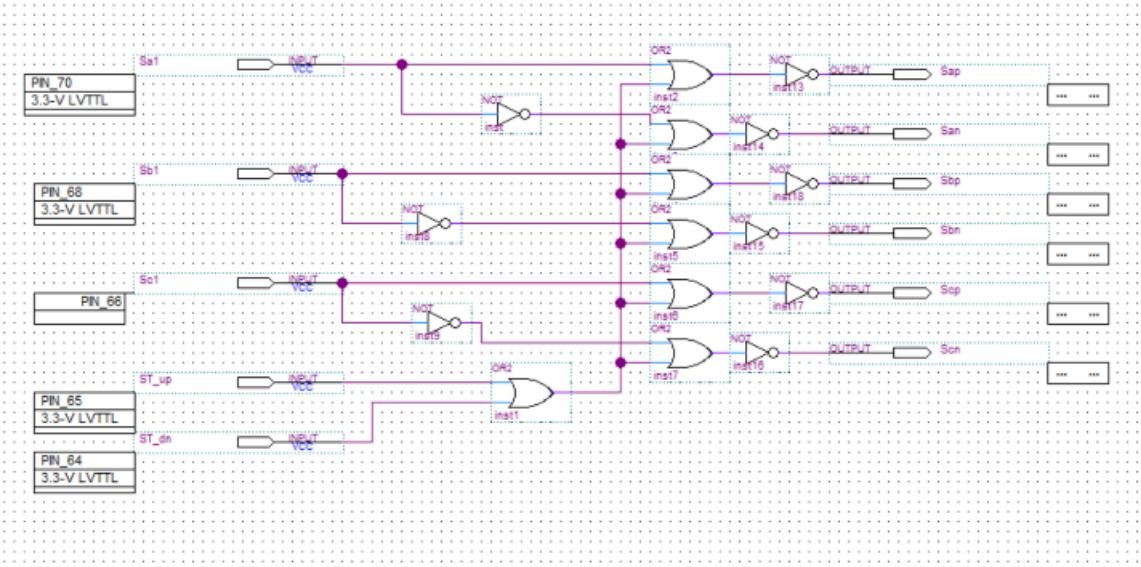


Figure 4.2: The program used in the FPGA.

- **DC source**: It offers an adjustable DC voltage, making it easy to modify the input voltage.
- **Load**: It is at the AC side and consists of three 3.07-mH inductors, acting also as a pure L filter with a 4.7-Ω resistor in Y connection.

The experimental setup is shown in Figure4.1.

4.1.1 Experimental Procedures

Two different control methods are tested in the experiments: the simple boost control (SBC), and the qZSI-modified space vector modulation in its 6-state shoot-through variant (ZSVM6). Three series of experiments are performed for each of the modulation methods in order to compare the obtained results when keeping both the modulation index M and the shoot-through duty ratio D constant. The test conditions are selected as:

1. $M = 0.6$, $D = 0.2$
2. $M = 0.8$, $D = 0.2$
3. $M = 0.8$, $D = 0.1$

With those conditions, the comparison between series 1 and 2 shows the effect of modifying the modulation index while keeping the shoot-through duty ratio

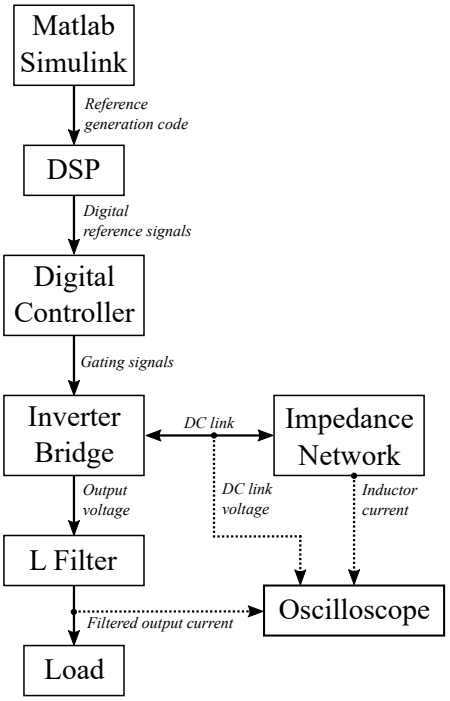


Figure 4.3: Block diagram of the experimental setup.

constant, while the comparison between series 2 and 3 shows the results of modifying the shoot-through duty ratio while keeping the modulation index constant. In all cases, the switching frequency of the inverter IGBTs is kept at 5 kHz, and the DC input voltage is maintained at 20 V.

In the experiment of the SBC, at the first step, the generation of the reference signals for both the traditional PWM and the reference shoot-through constants is performed in *Matlab Simulink*; making it simple to change the value of the shoot-through ratio D and the modulation index M. The reference signals are then sent to the DSP through a USB link, where the signals are processed, after which they are transfered to the FPGA. The program in FPGA is shown in Figure 4.2. As previously mentioned, this program is only used for the simple boost control, as its purpose is to insert the shoot-through states to the standard PWM control, achieving the simple boost control; whereas the ZSVM methods already include the shoot-through states in the signal sent to the DSP. As shown in Figure 4.2, this simple program uses OR and NOT gates to insert the two shoot-through signals ST_{up} and ST_{dn} into the six PWM gating signals, resulting in the modified PWM of the simple boost control. In the case of the ZSVM6, the FPGA code is not used.

The six gating signals are then sent to the inverter package. However, the voltage signal from the FPGA is too low to drive the IGBT gates, so the PM75RL1A120 inverter uses a 24-V input to boost the voltage of the gating signals to 15-V, in order

to realize the gating function. A simplified diagram of the experimental setup is shown in Figure 4.3.

After connecting all the equipment together according to Figure 1.6, we use voltage and current probes to measure the current of L_1, the DC-link voltage, and the current at the AC side in the oscilloscope, and then record the measured data.

4.2 Experimental Results

After recording the experimental results of the three mentioned series and two modulation methods, the obtained data is imported to *Matlab* in order to undertake its representation and analysis.

4.2.1 Inductor Current

Figure 4.4 shows the inductor current for the three data series using the simple boost control, as shown in the legend of the figure. From the two cases with $D = 0.2$, it can be seen that increasing the modulation index from 0.6 to 0.8 makes the DC component of the inductor current almost twice as large, while its ripple remains constant. On the other hand, decreasing the shoot-through duty ratio from 0.2 to 0.1 while keeping the modulation index constant at 0.8 results in both the DC component and the ripple of the inductor current to become half as large. Therefore, there is also a correlation between the first and third data series, as they have the same DC component but the series with a higher modulation index and a lower shoot-through duty ratio has lower current ripples.

Therefore, the larger the shoot-through duty ratio is, the higher the ripple of the inductor current will be, as the inductors will reach higher levels of charge. The amplitude of the current ripple also depends on the modulation method that has been used, as the distribution of the shoot-through states within every switching period determines the level of charge that the inductor will reach. This can be seen in Figure 4.5, which shows that the inductor current ripple is considerably lower when using the ZSVM6 that when using the SBC. This is due to the fact that the ZSVM6 splits the shoot-through time of each switching semi-period into six parts, which results in more charge/discharge cycles in the inductors. Therefore, in each switching semi-period, there will be six charge/discharge cycles, unlike the SBC which only introduces one cycle per switching semi-period. Therefore, the inductor current ripple is much larger for the SBC. The six cycles shown in Figure 4.5 are not quite as clear to see with the measuring resolution as the ones for SBC, precisely due to the much lower amplitude of the ripple.

It should be noted that the data obtained from the second series of the ZSVM6

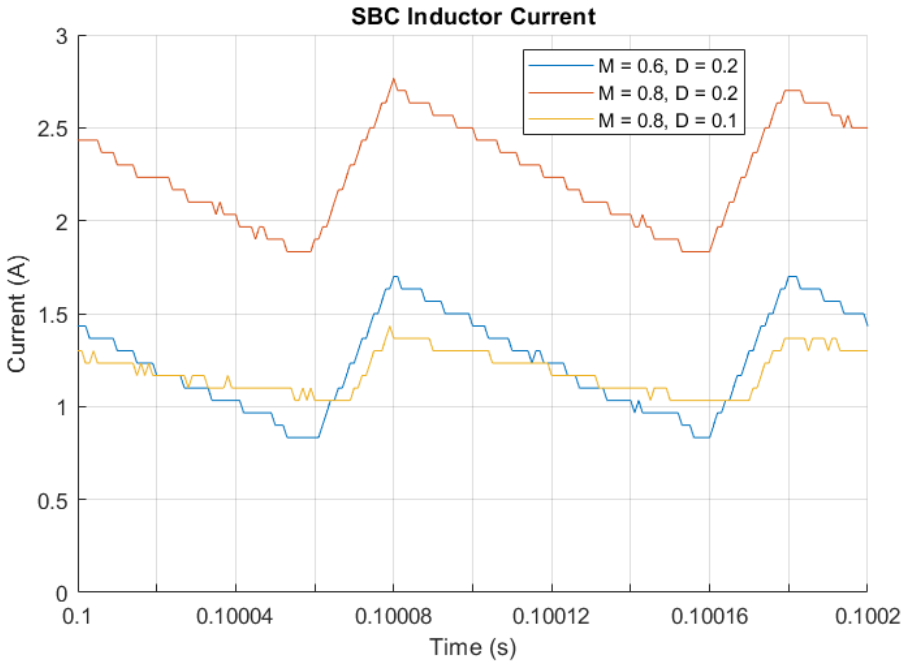


Figure 4.4: Current through the impedance network inductor of the three-phase qZSI with the SBC.

with $M = 0.8$ and $D = 0.2$ does not show the six charge/discharge cycles of the inductor, as with these parameters the inverter is not operating in continuous mode. This is also shown by the other ZSVM6 waveform results in Figures 4.8 and 4.11.

From Figures 4.4 and 4.5, it can be observed that at the shoot-through state, the inductors are charged, while at the non-shoot-through state, they are discharged, so the current increases at the shoot-through state and decreases at the non-shoot-through state. This can be observed more clearly in Figure 4.6, by also including the DC-link voltage, as this voltage approximately goes down to zero during the shoot-through states, and it can be seen that the zero DC-link voltage states correspond to the charging of the inductors, while the non-zero voltage states correspond to its discharging, thus boosting the voltage.

4.2.2 Output Current

From Figures 4.7 and 4.8, it can be observed that when the shoot-through duty ratio D is kept constant, the larger the modulation index M is, the higher the output current becomes. In a similar manner, when M is maintained constant, the output current increases with the increase of D. As the input voltage is 20 V, we

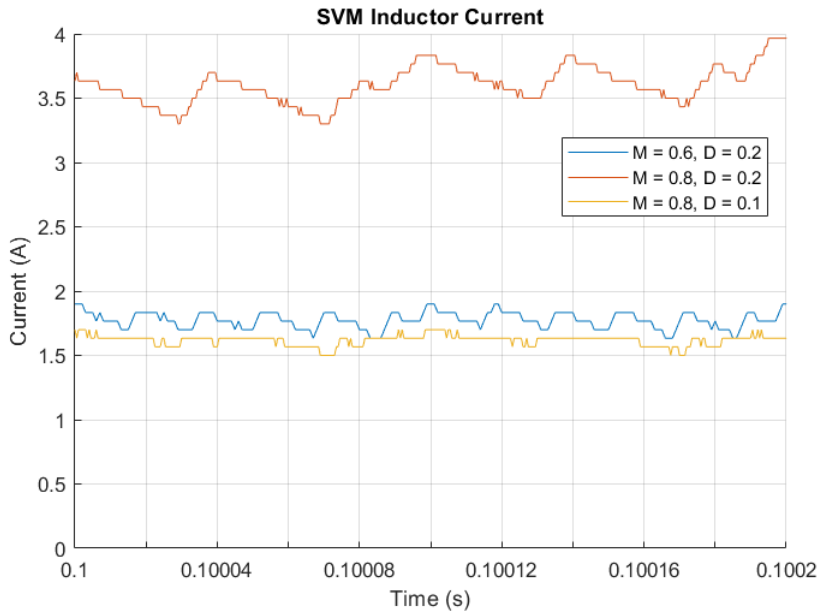


Figure 4.5: Current through the impedance network inductor of the three-phase qZSI with the ZSVM6.

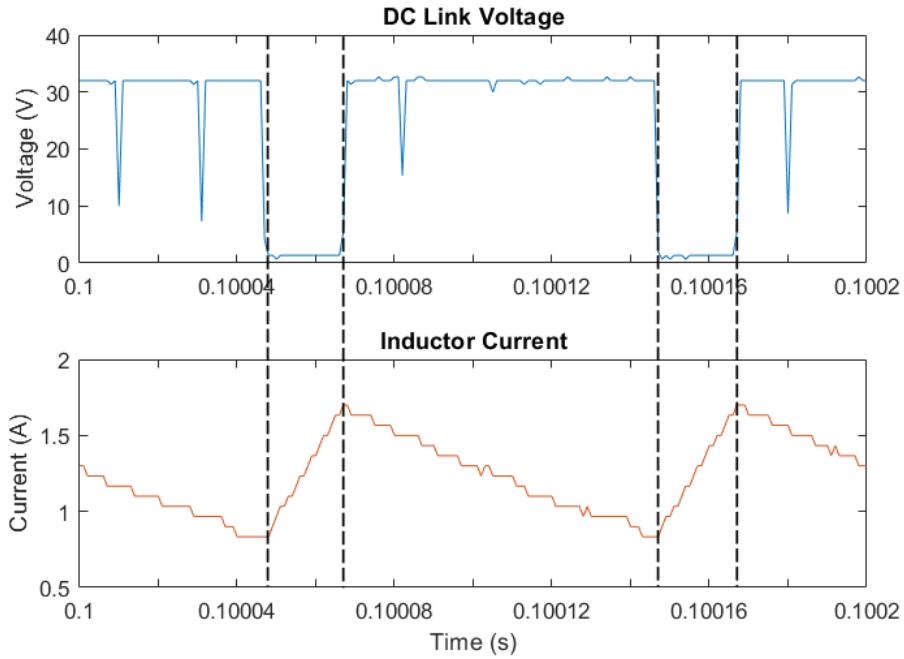


Figure 4.6: Visualization of the shoot-through states in the SBC.

can also verify the relationship between D, M and the peak of the output current:

$$I_{ac} = \frac{V_{in}M}{2(1-2D)R}$$

where R is the output Y-connected resistance rated at 4.7 Ω.

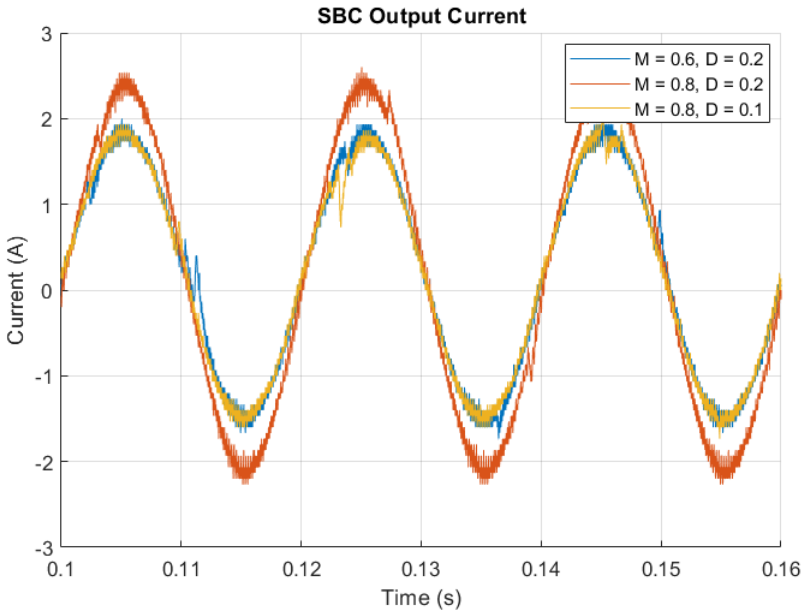


Figure 4.7: Output current of the qZSI with the SBC.

Figure 4.8 shows the distortion caused in the output current (and also the voltage, as a resistive load is adopted) by the non-continuous operation of the ZSVM6 with parameters $M = 0.6$ and $D = 0.2$. The current waveform also shows several spikes, mostly due to noise and measurement errors.

The distortion can also be shown in the frequency domain as presented in Figure 4.9. Figure 4.9 shows the frequency response of the output current data using a fast Fourier transform (FFT) algorithm, plotting the corresponding response to the data series containing larger output distortion ($M = 0.8$ and $D = 0.2$) together with that of a non-distorted output signal ($M = 0.6$ and $D = 0.2$).

Figure 4.9 shows that there is a clear current peak at the fundamental output frequency of 50 Hz, corresponding to the amplitude of the fundamental sinusoidal signal. The next most noticeable amplitude peaks are located at the frequencies of 250 Hz and 350 Hz, corresponding to the 5^{th} and 7^{th} harmonics, and associated with the insertion of shoot-through states. These harmonic components become larger in amplitude when the shoot-through duty ratio is higher, and also appear in the overmodulated SVM operation. Other low-frequency harmonics, most notably the 2^{nd} and 3^{rd} also appear in the spectrum, but with considerably lower

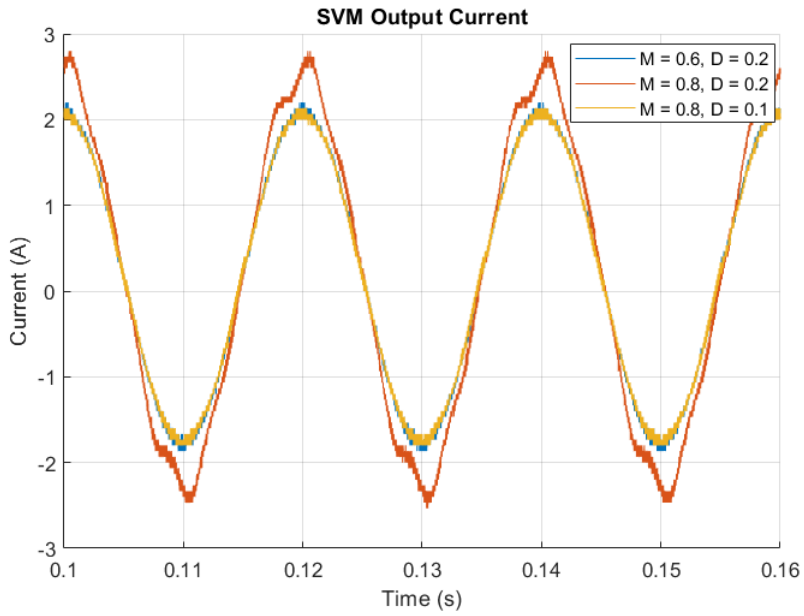


Figure 4.8: Output current of the qZSI with the ZSVM6.

amplitudes than the 5^{th} and 7^{th}. The frequency spectrum corresponding to the distorted data series clearly shows a much larger amplitude of the 5^{th} and 7^{th} harmonic components than the non-distorted data, resulting in the less ideal sine wave shown in Figure 4.8. The fundamental amplitude component is, however, boosted further in the distorted data than in the non-distorted data, although not as much as it would be boosted ideally.

4.2.3 DC-link Voltage

From Figures 4.10 and 4.11, it can be checked that at the non-shoot-through state, the relationship between D and the DC-link voltage is the following, as derived in chapter 2:

$$V_{PN} = \frac{V_{in}}{1 - 2D}$$

The DC-link voltage increases with D increasing, while at the shoot-through state DC-link voltage is zero. Figure 4.10 shows that there are two large voltage dips, corresponding to the shoot-through states, for each switching cycle of 0.2 ms. Compared to both inductor and output currents, the DC-link voltage depends only on the shoot-through duty ratio and not on the modulation index, as the modulation is only utilized after the DC-link in the switching legs of the inverter.

For the ZSVM6 simulation, the six voltage dips per switching semi-period of

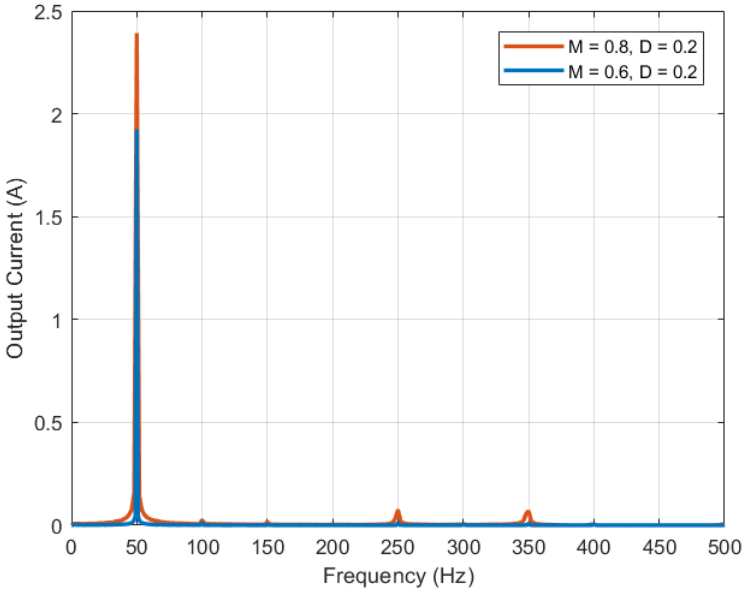


Figure 4.9: Fast Fourier transform of two output current data series for the ZSVM6.

0.1 ms can be seen for the first and third data series. The second data series, however, is not operating in the continuous mode, and thus shows only five dips. According to the space vector modulation analysis carried out in Chapter 3, this is due to the fact that the zero dwell time is not large enough to completely fit the shoot-through time that would be inserted in it, as the modulation index is too high for such a method. Although according to the results from Table 3.4 and Figure 3.20 a modulation index of 0.8 should allow for a ZSVM6 shoot-through duty ratio of up to approximately 0.3384, the experimental results show that the chosen value of $D = 0.2$ is too large for the used experimental setup, resulting in the non-continuous operation.

Therefore, the real shoot-through duty ratio received by the inverter is lower than the established 0.2, and the DC-link voltage does not reach the level that it theoretically should.

Table 4.1: Comparison of results for the average DC-link voltage using the SBC.

Parameters	Theory	Simulations	Experiments
$M = 0.6$, $D = 0.2$	26.67 V	27.28 V	25.36 V
$M = 0.8$, $D = 0.2$	26.67 V	26.61 V	24.94 V
$M = 0.8$, $D = 0.1$	22.50 V	22.48 V	21.43 V

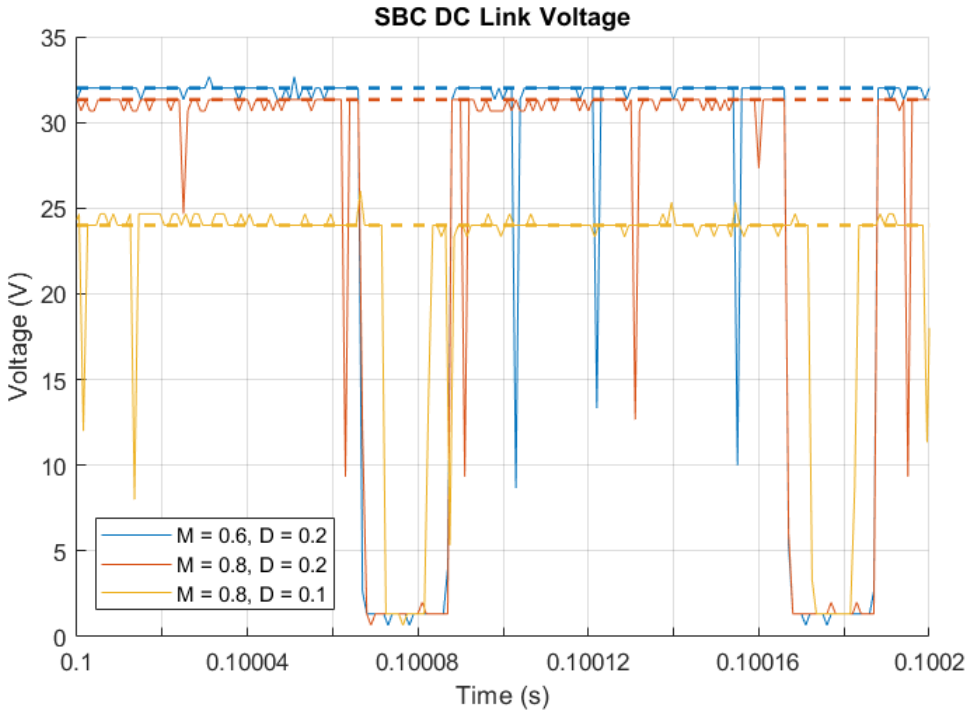


Figure 4.10: DC-link voltage of the qZSI with the SBC.

Tables 4.1 and 4.2 show the DC-link voltage results for the simple boost control and ZSVM6, respectively, comparing them with their corresponding theoretical and simulation results. Both tables confirm the accuracy of the simulation models, as the obtained results match the values predicted by the theoretical analysis. There is one exception, however, with the first data series ($M = 0.6$, $D = 0.2$) of the simple boost control. After analyzing the simulated waveforms, we have found a discontinuity in the DC-link voltage, resulting in part of the shoot-through state not reaching the null voltage. Consequently, the average DC-link voltage rises. This occurs due to the fact that the switching frequency is not large enough for use with the chosen modulation index. The phenomenon stops occuring when increasing either the switching frequency or increasing the modulation index, and it does not appear in the other data points, as validated in the simulations.

The experimental results show a clear trend to be lower than the theoretical and simulation results by between 1 V and 2 V, approximately, due to the non-ideal behavior of the experimental setup. There is another exception to this trend, appearing in the second data series ($M = 0.8$, $D = 0.2$) of the ZSVM6 control. In this point, the experimental voltage is lower than expected, due to the non-continuous operation explained previously in this section. As the shoot-through time does not last as long as it is intended, the DC-link voltage does not reach its

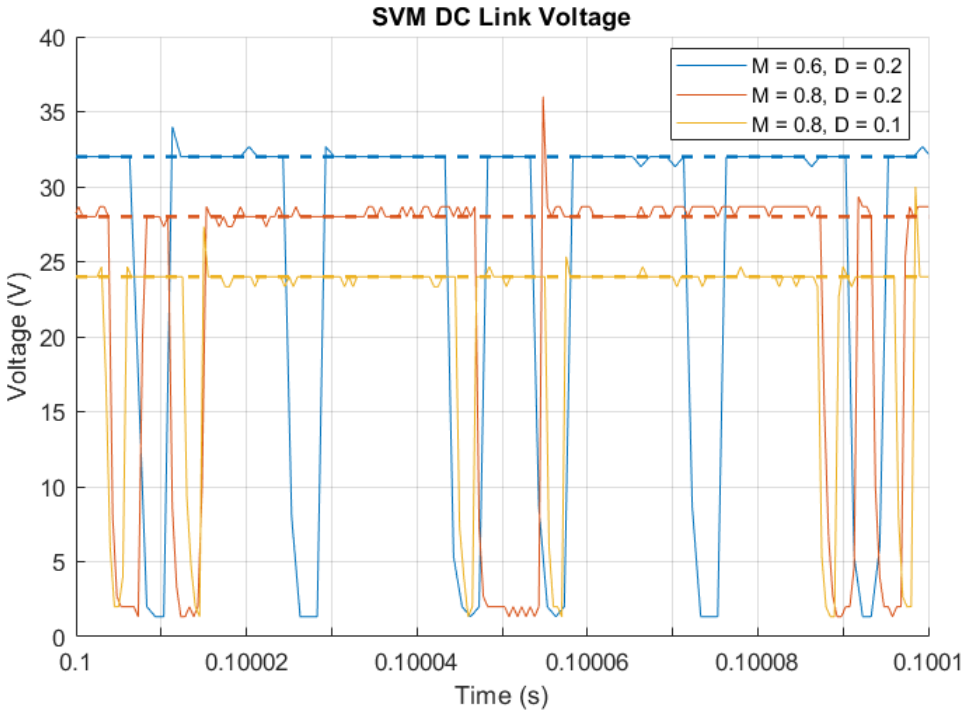


Figure 4.11: DC-link voltage of the qZSI with the ZSVM6.

expected value either.

For the simple boost control method, Table 4.1 shows a similar result for the first two data series, as they share the same shoot-through duty ratio. It is predicted that their DC-link voltages should be equal. Although the result is not exact, it can be affirmed that this prediction is confirmed. The same equality would be expected for the ZSVM6, as shown in Table 4.1. However, due to the previously mentioned discontinuity, this result is not confirmed by the experimental tests.

4.3 Summary

From the experimental results, the differences between the SBC and the ZSVM6 can be obtained. Figure 4.12 shows the current through the inductors in the Z-source network. It is clear that with the ZSVM6, there are less current ripples, as the ZSVM6 divides the shoot-through state into six parts per half-cycle, while the SBC only divides it into two parts per cycle. As the total time interval for the shoot-through state is the same, more shoot-through behaviors means that each time interval of shoot-through increases less for the ZSVM6 than for the SBC, causing comparatively less ripples.

Table 4.2: Comparison of results for average DC-link voltage using ZSVM6.

Parameters	Theory	Simulations	Experiments
$M = 0.6$, $D = 0.2$	26.67 V	26.67 V	25.29 V
$M = 0.8$, $D = 0.2$	26.67 V	26.63 V	23.94 V
$M = 0.8$, $D = 0.1$	22.50 V	22.49 V	21.4 V

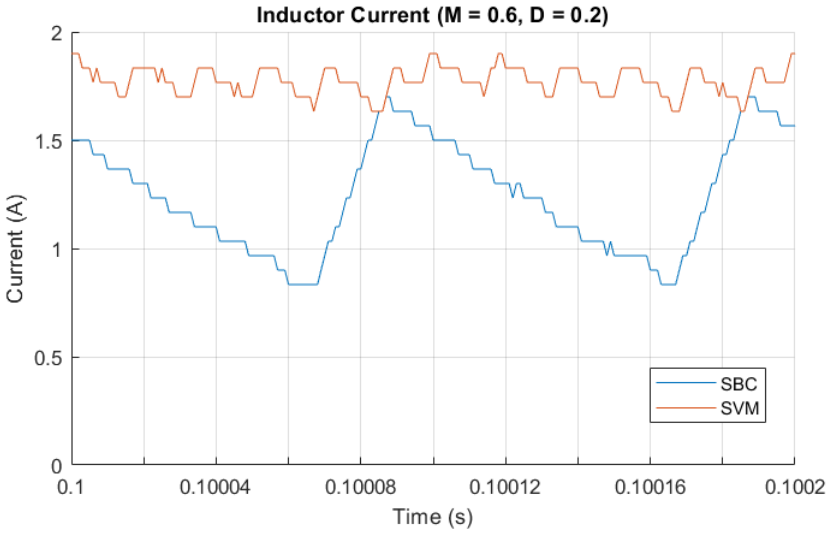


Figure 4.12: Comparison between the SBC and the ZSVM6 ($M = 0.6$, $D = 0.2$).

The average inductor current is also higher with the ZSVM6, as that method achieves better utilization of the DC input voltage. Moreover, the simulation results clearly show slight discontinuities appearing in the DC-link current and voltage, resulting in a slightly higher than the expected average DC-link voltage, but lower current. This is due to the fact that the used switching frequency of 5 kHz is not large enough to reliably insert the shoot-through states when using the carrier-based SBC. Although the resolution of the experimental results is not enough to fully verify this phenomenon, the same can be assumed to happen.

Another contributing factor to the SBC output current being lower than that of the ZSVM6 is that in the ZSVM6, the state of every switch just changes twice per switching cycle, as in the traditional PWM control, by only adding the shoot-through states to the existing switching times; while with the SBC all the switches are turned on during the shoot-through state, leading to more changes of switch states and increasing the losses for the SBC.

In Figures 4.13 and 4.14, we compare the simulation and experimental results of the output current with the SBC and ZSVM6, respectively. The parameters used

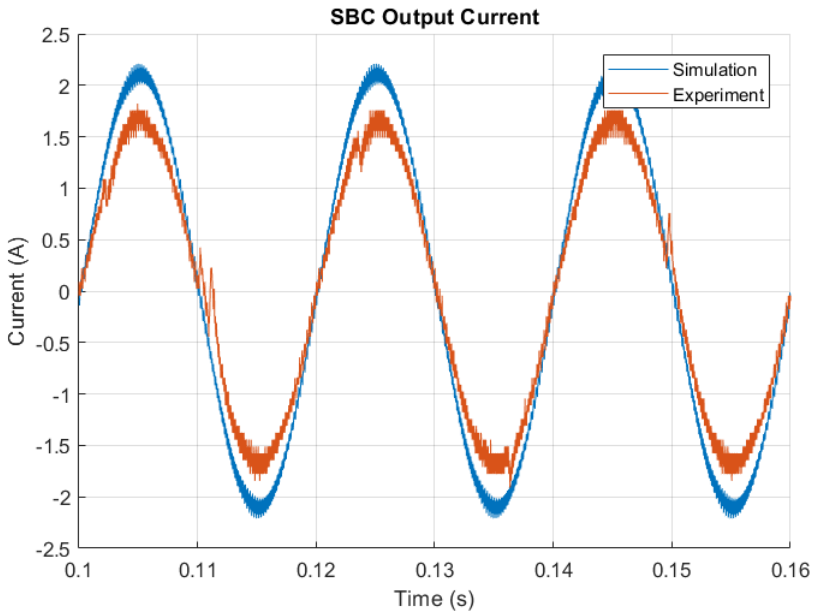


Figure 4.13: Comparison of the SBC output current with simulation and experimental tests ($M = 0.6$, $D = 0.2$).

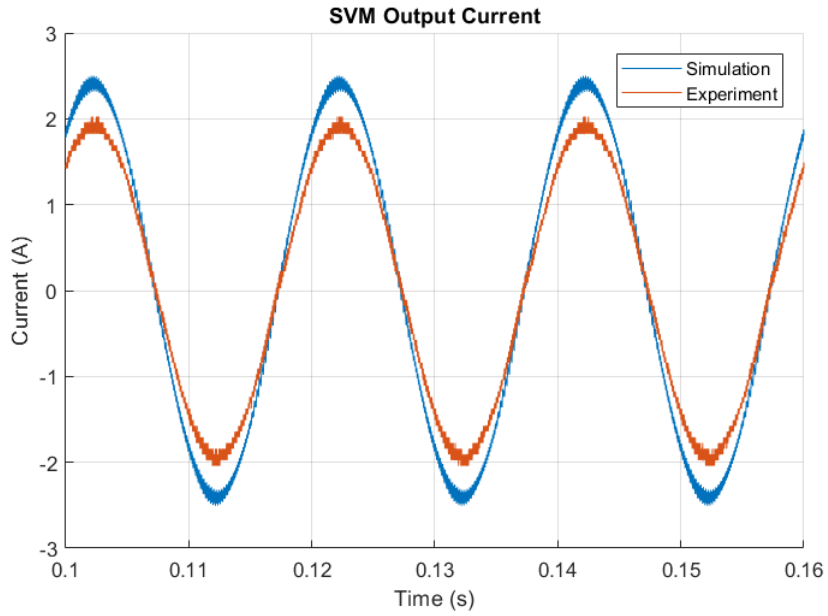


Figure 4.14: Comparison of the ZSVM6 output current with simulation and experimental tests ($M = 0.6$, $D = 0.2$).

for this experiment are: input voltage $V_{in} = 20$ V, load resistance $R = 4.7\ \Omega$, shoot-

through ratio $D = 0.1$, and modulation index $M = 0.8$. The simulation results of these two control methods differ significantly from those of the experimental tests. This is due to the fact that the used simulations assume all components ideal to verify the correct operation of the implemented modulation schemes. Therefore, no series or parallel resistance has been considered for the passive components, the switches have been considered ideal, and no forward voltage has been included in the diode. Therefore, the simulation results for the output current can be expected to show larger values than those of the experimental tests.

It is also noticeable that both simulation and experimental results show significantly smaller ripples in the output current signal for the ZSVM6 than for the SBC, as they are directly linked with the inductor current. Thus, the reason behind the lower inductor current ripple in the ZSVM6 can also be applied for both the output current and the output voltage.

Chapter 5

Conclusion and Future Work

5.1 Discussion

During the development of this project, we have made several decisions which have had an important impact on the final result. This chapter aims to explain these decisions and the reasons behind them.

- After studying several different types of impedance-source networks, we decided to focus on the quasi-impedance-source, as it is a solid improvement on the original X-shaped impedance-source without requiring any additional components. We wanted to avoid the use of coupled inductors and capacitors, as these can considerably increase the complexity of the system by introducing magnetic behaviors. The quasi-Z-source requires only two capacitors, two inductors, and a diode, all readily available power electronics components. The main advantages offered by this topology over the original Z-source are the achievement of a continuous input current and providing a common negative DC rail. Both of these advantages make the quasi-Z-source an adequate option for use in PV installations, without complicating the design of the impedance network. Therefore, the quasi-Z-source was the topology chosen for the designed impedance network.
- The project is also based on the study of three-phase inverters. In a traditional PV system, there are two components that can make use of the voltage-boosting capabilities provided by an impedance source. These are a boost-capable DC-to-DC converter and an inverter, which can be single- or three-phase. Although the impedance source could be added to the DC-to-DC converter, the inverter is the component that can benefit the most from the addition of an impedance source. This is due to the fact that traditional voltage-source inverters always generate an output AC voltage that has a

lower value than that of the DC input voltage. Therefore, the addition of an impedance source allows the inverter to operate as a buck-boost inverter, and effectively eliminating the necessity of a DC-to-DC converter between the power source and the inverter input. The inverter has been chosen to be three-phase because three-phase inverters are more efficient than their single-phase counterparts, by requiring six switching devices for three phases instead of four switching devices for a single phase. Three-phase inverters also allow for simpler analysis and control.

- All the analysis that has been carried out for the qZSI always assumes in steady-state operation. We have chosen to not focus on transients states because they greatly complicate the analysis of the inverter while not being indispensable for the development of control methods and design of passive components. A frequency domain model of the qZSI has not been developed for the same reasons.

- The control methods selected for study, simulation, and experimental tests are all based on pulse width modulation, because it currently is the most commonly used technique for power converter control and is able to yield the desired results with good performance. Carrier-based and space vector PWM have been chosen as the studied techniques for the very same reasons.

- Although simulations have been developed for all of the control methods presented, not all of the obtained results are shown in the report. This is due to the fact that all the obtained methods required for a thorough comparison between the methods have been considered to take up too much space for the amount of information they provide. Hence, the comparison between methods has been based instead on the theoretical analysis of the different methods, resulting in their ideal expressions.

- The developed simulations do not take into consideration any losses in the components due to non-ideal behavior, as we have thought it more illustrative to compare the experimental results with the ideal simulation ones, and thus visualizing the losses occurring in the experimental setup with respect to its ideal behavior. That is, no thermal behavior has been simulated for the system either, as the design of heat dissipation systems for the experimental setup is out of the scope of this project.

- For the experimental tests, only two of the analyzed control methods have been used: the carrier-based simple boost control and the space vector-based ZSVM6. Simple boost control has been chosen due to its simplicity for implementation and offering a good baseline for the comparison of results. The ZSVM6 has been chosen due to being the possibly most complex method to implement, but also offering much better performance by minimizing both inductor ripple and switching losses.

- Although criteria for the design of the passive components of the impedance network have been provided in the presented report, the parameters used in experimental tests have been chosen due to being readily available in the lab, after verifying that they comply with the aforementioned criteria and yield good results in simulation tests.
- Three data points have been chosen for the experiments:
  - $M = 0.6$, $D = 0.2$
  - $M = 0.8$, $D = 0.2$
  - $M = 0.8$, $D = 0.1$

  These parameter groups have been chosen to be able to compare results when modifying the shoot-through duty ratio at a constant modulation index and when modifying the modulation index at a constant shoot-through duty ratio. As observed in the experimental results, the second data point also causes the inverter to not operate in the continuous mode even though the theory presented in Chapter 3 suggests that it should, providing another source of comparison between experiments and theory/simulations.

5.2 Conclusion

The research object of this report is an improvement on a core component in a PV power system: the impedance-source inverter. In the three-phase inverter of PV systems, using a Z-source inverter to replace the traditional voltage source inverter can allow the system to overcome many of the shortcomings and limitations of the traditional inverter, improving the performance, flexibility, and reliability of the PV power system. After an extensive literature review, we have mainly done the following work:

- In Chapter 1, an introduction was presented on the current research on Z-source inverters for PV power systems. By analyzing the shortcomings of traditional inverters, the Z-source inverter was presented by F. Z. Peng which can solve many of the shortcomings of traditional inverters. The working principle of the Z-source inverter is explained in detail. Also, several types of impedance networks are compared, while mainly focusing on the quasi-ZSI, which is the topology on which simulations and experiments are based.
- In Chapter 2, according to the analysis of the two working states of the qZSI, the expressions defining the voltage and current of the different components of the qZSI are derived. Thus, the relationship between the input voltage and

output voltage is found, defining the voltage-boosting ability of the quasi-Z-source inverter. Also, the expressions for the ripple of the capacitor voltage and inductor current of the quasi-Z-source network have been deduced, with which the capacitance and inductance can be designed, together with the voltage and current ratings they are submitted to. An example of the single-phase qZSI is shown based on the modeling and analysis, for which the model of its impedance network is more complicated than that of the three-phase qZSI. According to these mathematical models, we can estimate the parameters that should be used in the experimental tests, offering a theoretical basis for the selected components.

- In Chapter 3, based on the analysis of the traditional carrier-based PWM modulation strategies, several modifications on the traditional method are discussed, which share the objective of introducing the shoot-through states to the inverter in order to boost output voltage as desired. Three modified carrier-based PWM methods are described: the simple boost, maximum boost, and maximum constant boost methods; all of them modified with a shoot-through signal that can be applied to the three-phase Z-source inverter. Four modified space vector modulation methods, ZSVM6, ZSVM4, ZSVM2, and ZSVM1 are also illustrated in this Chapter. These control strategies for the qZSI are studied theoretically, and their differences are discussed in detail. According to theoretical research, simulations have been developed to verify each of the different control schemes.

- In Chapter 4, the equipment and circuitry used in the experiments is presented. According to the discussions in chapter 3, simulations based on the carrier-based simple boost control and the ZSVM6 are built up to control the circuits, interfacing with the inverter circuit through a DSP and FPGA. The experimental results verify the theories and expressions derived in the previous chapter.

The quasi-Z-source inverter is a modification on existing inverter technology that uses a unique impedance network to couple the power source and the power conversion circuit. By adequately designing this impedance source, several performance improvements are achieved. Mainly, it allows the inverter to boost the output voltage, while traditional voltage-source inverters can only operate as buck inverters. On the other hand, traditional current-source inverters can only boost the voltage, while the addition of the impedance source allows them to buck it. Another advantage presented by the impedance-source inverter is its ability to be short-circuited, thus boosting the voltage without damaging the switching devices; which in traditional inverters represents a source of lifespan shortening.

Therefore, it has the advantages over conventional inverters of being able to not only reducing output voltage with respect to the input, but also being able to boost

it. This is desirable in PV power systems, where the DC power generation from the PV panel array is often lower than the desired output AC voltage. Therefore, the currently most common topology used in PV power systems is using boost DC-to-DC converters between the power source and the inverter. The impedance-source inverters can, by making use of their voltage-boosting ability, eliminate the need for such intermediate converters, thus resulting in increased system efficiency and simplicity, as well as lower costs. On the other hand, the passive components required for the impedance network can be considerably bulky, and undesired low frequency harmonic components can appear in the output signals more commonly than when using traditional inverter topologies. However, the increased reliability and flexibility that impedance-source inverters add to traditional PV power systems can make them a compelling choice in the future.

5.3 Future Work

This project has carried out basic theoretical analysis, together with simulation and experimental verification for the qZSI. There are still many topics that need to be further studied and discussed:

- This project has only focused on the qZSI variant of impedance-source converters. Therefore, more research should be undertaken on the comparison between different impedance network topologies and the use of impedance networks in other types of power converters. A comparison between voltage-source and current-source topologies could also be developed.
- This report only studies the working principle of the qZSI in the continuous operation mode, and does not analyze the situation in the DCM (Discontinuous Conduction Mode). These two states have completely different working characteristics.
- The circuit analysis carried out for the qZSI assumes in steady-state operation, and transient performances are not considered. These states are often very relevant to the design of circuit components, as they are usually subjected to highest stress during transients.
- Other modulation methods, including the ones introduced in the control section of the presented report, should also be tested in the lab, which in this case was limited to only the carrier-based simple boost control and ZSVM6.
- For the design of hardware and software, only a brief introduction is presented, and further research is needed on the coordination and reliability of the whole circuit.

- Because of time limitations, this paper is only focused on open-loop control. In order to improve the performance of the system, one or several control loops should be added to the control system. The closed-loop control can compensate for variations in the input voltage, which is a very desirable advantage in a PV power system. Control loops can also be designed to minimize undesired harmonics in the output current and voltage [3].

- Another fundamental characteristic required for an efficient Z-source inverter-based PV power system is to include maximum power point tracking techniques to maximize the input power from the PV panels. Therefore, a control loop should also be included to include such a technique in the inverter control.

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Appendix A

Simulation Results

The results for the DC-link voltage obtained from the modified space vector modulations are shown in this appendix, as we have thought it appropriate to include them as a means to verify the developed models. The results clearly show the differences between the ZSVM methods, and also confirm the expected theoretical results.

A.1 Modified Space Vector Pulse Width Modulation

Figure A.1 shows the *PLECS* simulation results for DC-link voltage when using the five analyzed modified SVM methods (counting ZSVM1-I and ZSVM1-II separately). All the results shown use the same parameters are the first data point of the experimental tests. These are, as described in chapter 4:

- Impedance network inductors: $L_1 = L_2 = 300$ μH.
- Impedance network capacitors: $C_1 = C_2 = 200$ μF.
- Y-connected load resistor: $R_L = 4.7$ Ω per phase.
- Output L filter inductance: $L_f = 3.07$ mH per phase.
- DC input voltage: $V_{in} = 20$ V.
- Switching frequency: $f_s = 5$ kHz.
- Shoot-through duty cycle: $D = 0.2$.
- Modulation index: $M = 0.6$.

All components have been considered ideal, not considering any resistive losses in any of the components and assuming zero forward voltage for the diodes.

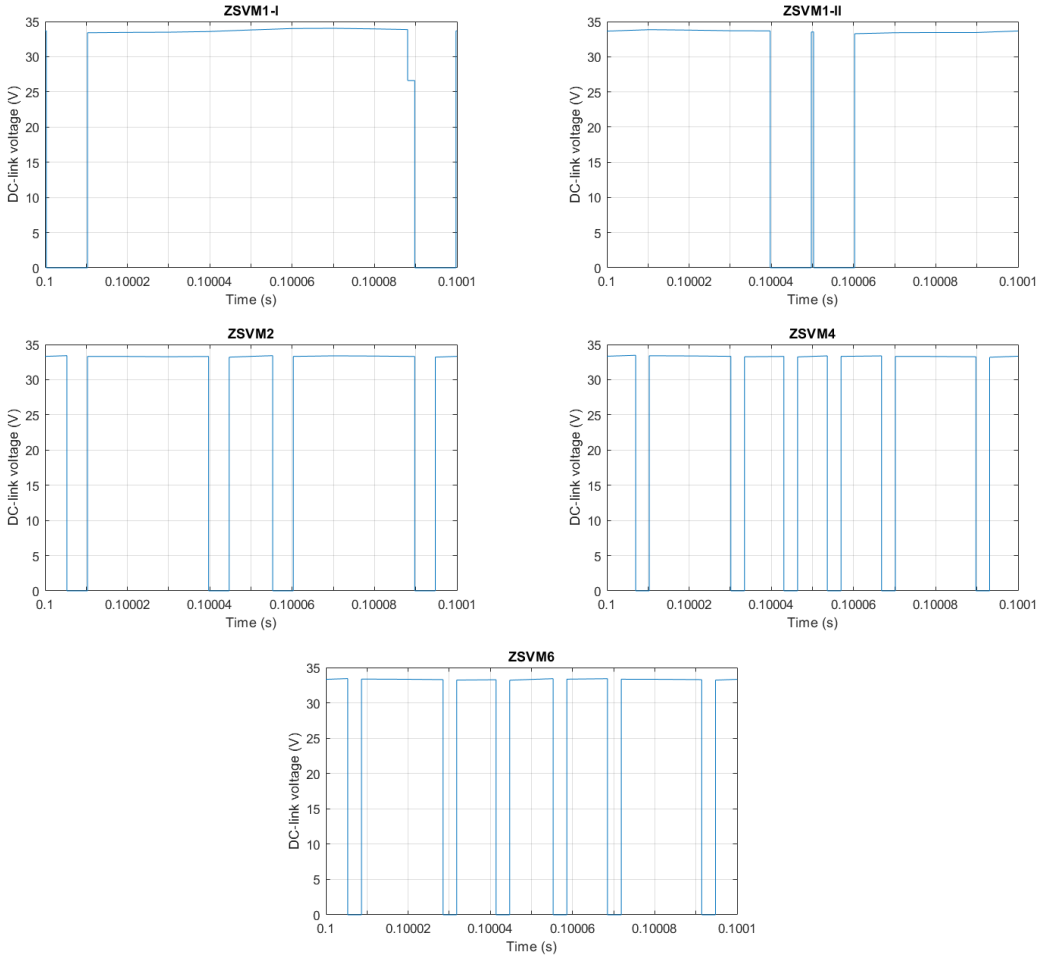

Figure A.1: DC-link voltage simulation results using ZSVM control methods.

Figure A.1 clearly shows how each of the ZSVM methods inserts its shoot-through states. The shoot-through states correspond to the periods when DC-link voltage falls to zero, while the non shoot-through states correspond to the periods with boosted voltage.

Both ZSVM1 methods show the insertion of the shoot-through states in two separate segments. The distinction between ZSVM1-I and ZSVM1-II is also clearly visualized, as the shoot-through states are inserted in different positions as described in figure 3.19 of chapter 3. Although the shoot-through states appear in different positions within a switching cycle, both methods are effectively equivalent, as the spacing between the inserted shoot-through states is globally the same in both methods.

The waveform for ZSVM2 shows the division of the shoot-through time into four shoot-through states of the same duration, distributed as shown in figure 3.19.

The waveforms of ZSVM4 and ZSVM6 may appear equivalent at first glance, as both divide the shoot-through time into six periods of equal duration and present a similar distribution of these states. However, closer inspection shows that the time periods between shoot-through states are not equal, with ZSVM6 having the first shoot-through period earlier than ZSVM4, and the third shoot-through period later than ZSVM4; again, as shown in figure 3.19.

The simulations for modified space vector modulation confirm, thus, the results expected from the analysis of the control methods performed in chapter 3.